

EVALUATION OF RADIO FREQUENCY CMOS INTEGRATED CIRCUIT
TECHNOLOGY FOR WIRELESS LOCAL AREA NETWORK APPLICATIONS

By

XI LI

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Abstract of Dissertation Presented to the Graduate School
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By

Xi Li

May 2003

Chair: Kenneth K. O

Major Department: Electrical and Computer Engineering

Radio frequency (RF) and microwave communications market has enjoyed tremendous growth over the last decade. Wireless technology is now capable of reaching virtually every location on the face of the earth. Over the recent years, wireless Local Area Network (LAN) technology has emerged as a leader among technologies for wireless internet access.

Lowering the cost of wireless LAN (WLAN) hardware is critical in allowing the general public to have access to WLAN technology and push the technology for mainstream acceptance. To date, silicon-based processes have been the dominant technologies in developing WLAN chipsets due to their lower cost compared to compound semiconductor processes like gallium arsenide (GaAs) MESFET and HBT technologies. Presently, most of the RF integrated circuits (IC's) in the market are built using silicon (Si) bipolar junction transistor (BJT) or silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) technologies. Recent speed improvements of digital sub-micron bulk CMOS tran-

sistors have also made it feasible to implement RF circuits operating at 1 GHz and above in CMOS technologies. Potentially, by exploiting the economy of scale, CMOS technology could provide even lower cost solutions than the Si bipolar and SiGe HBT technologies. This dissertation evaluated the feasibility of implementing a 2.4-GHz transceiver for wireless LAN applications in a 0.25- μm CMOS process which has comparable over-all performance as a commercial SiGe HBT transceiver and developed understanding of observed differences.

CMOS low noise amplifier (LNA) and mixer are first designed and tested as these two receiver components usually have more stringent and challenging specifications. Their performance is compared to that of SiGe BJT LNA and mixer. It is shown that CMOS LNA and mixer can match the SiGe performance with a 15 to 20% increase in bias current, indicating that a full CMOS transceiver chip is feasible. CMOS and BJT RF circuits are compared at fundamental device physics level as well as process and manufacturing level. MOS and BJT device variations due to process and temperature are evaluated for RF tuned circuits with different Q values. Based on these discussions and LNA design experience, a unique design methodology, Q based design approach, is presented. It is believed that this approach can significantly reduce the risk of RF IC design. Next, a frequency synthesizer, which is the most complex component of the transceiver, is realized in the CMOS process. The desired frequency locking is achieved with phase noise close to that of the SiGe synthesizer. Finally the entire CMOS transceiver is designed, fabricated and characterized. All the circuit blocks on the CMOS transceiver are functional and their performance is close to that of the SiGe transceiver. The CMOS prototype chip is also incorporated in a commercial IEEE 802.11b WLAN system (PRISM II.5). For the

first time, PRISM II.5 WLAN with a CMOS transceiver is successfully demonstrated. The performance of the CMOS and SiGe radios is close with CMOS radio consuming 5% more current than that for the SiGe radio. The success of this dissertation points out the direction of higher integration and opens the door for many possible future works.

CHAPTER 1 INTRODUCTION

1.1 Wireless LAN Technology and Market

Radio frequency (RF) and microwave communications market has enjoyed tremendous growth over the last decade. Wireless technology is now capable of reaching virtually every location on the face of the earth. Cellular telephones, pagers and other various wireless products have become an important part of our everyday life. Since the success of the Ethernet project at Xerox's Palo Alto Research Center in the early 1970's [Met76] and other similar digital protocols, the local area network (LAN) technology has blossomed. Numerous LANs have been installed in both the public and private sectors around the world, forming one of the integral parts of the Internet. Standard LAN protocols, such as Ethernet, can operate at fairly high speeds with inexpensive connection hardware, bringing digital networking to almost any computer. A wireless local area network (WLAN) is a flexible data communications system implemented as an extension to, or as an alternative for wired LAN. Using RF technology, wireless LANs transmit and receive data over the air, minimizing the need for wired connections. Therefore, wireless LAN technology is able to combine data connectivity with user mobility, and offer simple and flexible network installation with reduced cost of ownership and enhanced network scalability. The WLANs are used in a variety of environments: "Vertical," which includes factory, warehouse, and retail; "Enterprise," which includes corporate and academia campuses;

“SOHO,” Small Office/Home office; and “Consumer,” emerging home networking and beyond [Lou97, Pav00].

In June, 1997, the Institute of Electrical and Electronics Engineers (IEEE) introduced the first internationally recognized standard for WLANs: IEEE 802.11. It serves the same purpose as the IEEE 802.3 standard for wired Ethernet: establishing standards for vendor to vendor interoperability. IEEE 802.11 specifies the physical layer and media access control (MAC) layer within a WLAN scheme. The MAC protocol is a scheme called carrier sense multiple access collision avoidance (CSMA/CA), similar to its IEEE 802.3 predecessor. Three physical layers were originally offered: direct sequence spread spectrum (DSSS), frequency hopping spread spectrum (FHSS) (both use 2.4 GHz ISM band), and infrared. In 1999, the IEEE 802.11 Wireless LAN working group ratified the 802.11b standard which delivers up to 11 Mb/s in the 2.4 GHz ISM band. Since then, IEEE 802.11b WLAN based products have formed the mainstream. Today, 802.11b based WLAN is penetrating into a number of new markets, including, coffee kiosks, airport terminals, and home networking.

1.2 Proposed CMOS Wireless LAN Transceiver IC

1.2.1 Integrated Circuits (IC's) for Wireless LAN

In order to deliver the WLAN technology, high integration and low cost are essential in reducing the bill of materials (BOM) for original equipment manufacturers (OEMs). Silicon-based RF process technologies can exploit the highly developed silicon technology with a larger wafer size (potentially 300 mm wafer diameter) to provide lower cost solutions in an operating frequency range where III-V compound semiconductor based technologies have traditionally dominated. As a matter of fact, silicon bipolar junction

transistor (Si BJT) and silicon-germanium hetero-junction bipolar transistor (SiGe HBT) technologies have emerged as the dominant force in this marketplace. Recent speed improvements of digital sub-micron bulk CMOS transistors have also made it feasible to implement RF circuits operating at 1 GHz and above in CMOS technologies. Potentially, by exploiting the economy of scale, CMOS technology could provide even lower cost solutions than the Si bipolar and SiGe HBT technologies. This Ph.D. research seeks to evaluate the feasibility of implementing a 2.4-GHz transceiver for wireless LAN applications which has comparable over-all performance as a SiGe HBT transceiver in a 0.25- μm CMOS process. Through this project, understanding of the performance limitations of CMOS and SiGe bipolar technologies for wireless applications will be developed and this understanding will be used to assess the breadth of applicability for CMOS technologies in communication applications.

1.2.2 Research Goals and Milestones

This Ph.D. work will develop a low noise amplifier (LNA), receive and transmit mixers, a frequency synthesizer, and a power amplifier driver operating at 2.4 GHz in a 0.25- μm CMOS process. These blocks will be housed in a 44 pin Micro Lead Frame (MLF) package and tested on the PC board for PRISM II.5. Finally, all the RF blocks will be integrated into one transceiver chip. The CMOS transceiver will be equivalent to the SiGe HBT transceiver. The prototype CMOS chip will be incorporated into a 802.11b wireless LAN radio and the whole system will be evaluated.

Since the CMOS transceiver is functionally equivalent to its SiGe counterpart, this research will provide a unique opportunity to make almost an apple-to-apple comparison of the capabilities of CMOS and SiGe HBT technologies for wireless LAN transceiver

applications. In addition, understanding of the limitations of RF circuit characteristics such as noise, linearity, gain, power consumption, signal isolation, process variations and others in CMOS and bipolar technologies will be developed and compared. These will be used to understand and explain the transceiver-level comparison results, and to assess the critical advantages of each technology.

1.3 Overview of the Dissertation

The dissertation focuses on the IC implementation of various RF blocks and transceivers in CMOS technology. In Chapter 1, the background and motivation of this research are presented. In Chapter 2, various IC technologies are introduced and their merits are compared for WLAN application. In Chapter 3, the overall RF system of a 2.4 GHz WLAN is discussed and the design of two receiver building blocks, LNA and mixer is presented. Their measurement results are compared to the ones of a commercial SiGe transceiver chip. In Chapter 4, BJT RF device of SiGe BiCMOS process and the MOS RF device of CMOS process are compared in terms of process/temperature variations. The impact of component variations in different IC technologies on RF tuned circuits with different Q values is assessed. In Chapter 5, using LNA design as an example, a unique design methodology, Q based design approach is developed and presented. It is believed that this approach will help to start the design on the right track and significantly lower the risk of RF IC design. In Chapter 6, the frequency synthesizer which is the most complex component of the transceiver is described. In Chapter 7, the design of the transmitter chain is discussed and the overall CMOS transceiver design is presented. In Chapter 8, the characterization of the CMOS wireless transceiver chip is shown and the radio level evaluation

of the WLAN system with the prototype CMOS chip is also demonstrated. In the last chapter, the Ph.D. work is summarized and the future work and direction are pointed out.

CHAPTER 2 IC TECHNOLOGIES FOR WIRELESS LAN

2.1 Technology Options

One of the main reasons behind the “explosion” of the wireless communications market in the 1990’s is the advance and development of IC technologies that deliver cheap and reliable RF circuits. RF applications like amplifiers, oscillators, mixers and other active circuits all depend on high quality transistors. Traditionally (before the 1980’s), these transistors are realized in a discrete manner. They are less reliable, occupy bigger board area and hard to integrate. A typical transceiver usually requires tens of IC’s and hundreds of discrete components which occupy a lot of real estate on the PC board.

2.1.1 Silicon RF Technologies

One of the greatest achievements of twentieth century civilization is the maturing and industrialization of silicon integrated circuit technology. In the late 1980’s, the silicon bipolar RF technologies were able to provide npn transistors with a transit frequency f_T of about 10 GHz to serve the basic transceiver function for cellular applications below 1 GHz. During the 1990’s, the f_T was improved to above 20 GHz [Sev00]. Fig. 2-1 shows a cross section of a modern RF Si bipolar junction transistor (BJT) featuring double poly base and emitter which significantly reduce the parasitic capacitances and resistances compared to the old technology shown in Fig. 2-2 [Nin01].

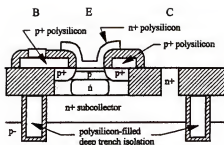


Figure 2-1 Double poly Si bipolar npn transistor

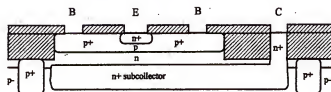


Figure 2-2 Conventional bipolar transistor, old technology

BiCMOS technology combines the npn bipolar technology and the mainstream CMOS technology to fabricate npn transistors used for RF application as well as nMOS and pMOS transistors used for digital circuitry on the same wafer. It offers the highest integration level in transceiver IC design and is believed to be a strong candidate for “Radio-on-chip” IC’s. Most of the companies that developed a npn RF bipolar process eventually went on to build a BiCMOS process around the npn transistor. A pure bipolar process is becoming obsolete due to its limitation of the level of integration. There is a 20 to 30% cost increase for BiCMOS compared to a pure CMOS process.

Research in epitaxial techniques such as chemical vapor deposition (CVD) in the eighties had prompted the development of a silicon hetero-junction bipolar transistor (HBT) structure, namely, the silicon-germanium bipolar transistor (SiGe HBT). By introducing germanium (Ge) into the npn base region, as shown in Fig. 2-3, performance of 50

GHz f_T can be easily realized. A great advantage of SiGe technology is that, it is fully compatible with the main stream CMOS process. This makes it very attractive to silicon foundries around the world and SiGe BiCMOS has become the dominant RF technology.

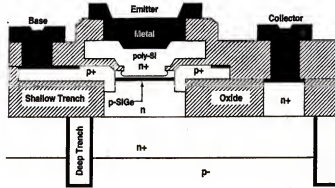


Figure 2-3 A cross section of SiGe HBT [Har95]

Besides Si and SiGe, Lateral Double Diffused MOS (LDMOS) is another Si RF technology. However, it is not widely accepted and its use is confined only to power circuits. CMOS process technology, on the other hand, is most available. It has become increasingly promising for RF applications and that is the main reason for this research.

2.1.2 GaAs Technologies

Many important applications such as optoelectronics and millimeter-wave devices are best suited with compound semiconductors. Their physical properties, most notably large and direct bandgap and high electron mobility, make them unique in applications where use of silicon is currently not possible. Traditionally, GaAs (gallium arsenide), a III-V compound semiconductor (III-V means it is a binary compound because it consists of two different elements, gallium from column III and arsenic from column V of the periodic table), has been well established as a common material for commercial MMIC's at

frequencies above 1 or 2 GHz [Goy95]. Other III-V compounds like GaP, InP, InSb and GaN are also interesting materials for applications in a wide frequency range from millimeter-wave to blue light.

To date, GaAs is still a semiconductor material second to silicon. It has two basic advantages over silicon: first, a semi-insulating substrate that allows fabrication of high quality passive components and better active devices with less parasitic capacitances; second, a higher electron mobility that makes electrons move faster, consequently enables device operation at higher frequencies. It, however, has a few disadvantages: poor native oxide, high defect density, mechanical fragility, etc. All these lead to low yield, low integration level thus high die cost [Goy95].

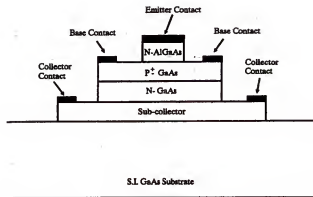


Figure 2-4 GaAs HBT

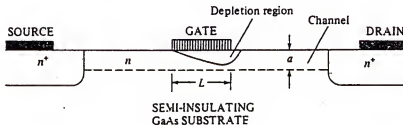


Figure 2-5 GaAs MESFET

There are two GaAs processes that are commonly used in RF applications: GaAs HBT, and GaAs MESFET. Fig. 2-4 and 2-5 illustrate these two technologies.

2.2 Figures of Merit of Various RF IC Technologies

The optimum RF IC technology choice is still a subject of heated debate [Goy95, Lar96, Mon97, Lar98, Ulf98, Sev00]. The ultimate figures of merit may be the cost and time to market which are determined by a wide variety of factors, including yield, integration level, process availability and even engineering resources. Most commercial implementations of wireless systems are realized in a mixture of technologies these days. The key transistor technology figures of merit for RF and microwave applications are unity current gain frequency f_T , maximum power gain frequency f_{max} , minimum noise figure, $1/f$ noise corner frequency, maximum power added efficiency (for power amplifier), linearity, and reliability.

Table 2-1 lists some typical figures of merits of Si and GaAs technologies. These numbers are constantly evolving as the technology advances. The Si BJT/BiCMOS process quoted here is Intersil UHF2 0.6- μm BiCMOS process [Hem00]; the SiGe process quoted here is an IBM 0.25- μm foundry process [Har01]; GaAs data are from Moniz [Mon97] and CMOS data are from Chew et al. [Che01].

For Wireless LAN applications at 2.4 GHz ISM band, these technologies are all adequate in terms of speed and noise. Silicon technologies are clearly the choice here because of their lower cost and higher level of integration. The question is which Si technology should be used, BJT/BiCMOS or CMOS? Both Si BiCMOS and SiGe BiCMOS technologies have been employed in designing the commercial chipset at a leading Wire-

less LAN semiconductor company. It is the purpose of this Ph.D. research to find out whether CMOS technology is suitable for the same task.

Table 2-1 Typical Figures of Merit of Various RF IC Technologies

	Si BJT/ BiCMOS	SiGe BJT/ BiCMOS	GaAs HBT	GaAs MESFET	Si CMOS
Feature Size	0.6 μm	0.25 μm	2 μm	0.5 μm	0.25 μm
Peak f_T	27 GHz	47 GHz	50 GHz	30 GHz	~ 40 GHz
Peak f_{max}	37 GHz	65 GHz	70 GHz	60 GHz	~ 50 GHz
Minimum N.F. @ 2GHz	1.0 dB	0.5 dB	1.5 dB	0.3 dB	~ 1.5 dB
1/f noise corner	$10^2 - 10^3$ Hz	$10^2 - 10^3$ Hz	1-10 kHz	~ 10 MHz	~ 1 MHz
Breakdown $BV_{\text{ceo}}/BV_{\text{ds}}$	3.8 V	3.35 V	15 V	10 V	~ 3-5 V

2.3 BJT and MOSFET Device Physics Comparison

We have narrowed it down to two candidate IC technologies for WLAN applications: silicon BiCMOS technology (including SiGe BiCMOS) and silicon CMOS technology. It is the high speed devices in these two technologies, i.e., the npn bipolar junction transistor (BJT) and nMOSFET device that determine the performance of RF circuits.

Before we embark on the task of comparing MOSFET and BJT circuits for RF application, it is prudent to briefly visit the fundamental physics of these two devices. The operation of BJT's is based on the physics of junctions (pn junctions) while MOSFET's are basically field (voltage) controlled conductors. Table 2-2 compares the basic characteristics of BJT and MOSFET devices. In Appendix A, these two devices are examined from a very fundamental physics point of view.

Table 2-2 Device Physics Comparison of BJT and MOSFET

	BJT	MOSFET
Carriers	Minority Carriers	Majority Carrier
Current Mechanism	Diffusion Current	Drift Current
I-V Characteristic	Exponential	Square Law
Major Noise	Shot noise	Thermal noise
Oxide	No	Yes
1/f noise	small	large due to the presence of oxide

2.4 Why RF CMOS?

Why RF CMOS? Can and will CMOS replace bipolar transistors in all analog and RF applications? Will bipolar technology be obsoleted? These are the questions that have been asked in numerous conferences for the past few years [Gil98]. Often this stirs up emotional debates between bipolar aficionados and CMOS evangelists. Until now, there is no sign that these questions or debates will go away in the near future and certainly merit discussions.

2.4.1 Availability and Accessibility

Without a question, CMOS is the most available and accessible process among all semiconductor IC technologies. A wide range of CMOS processes are offered by semiconductor foundries around the world. CMOS is the absolute technology choice for most digital applications which comprise the majority of annual worldwide semiconductor sales. Because of this, CMOS will continue to be the dominant technology for decades to come. And that is the No. 1 advantage of CMOS process over Bipolar or BiCMOS and the main reason behind "RF CMOS." The dominant position of CMOS will also bring other

advantages as well, for example, largest pool of engineering resources and capital investment.

2.4.2 Cost, Yield and Integration Level

The main appeal of CMOS preached by its advocates is its relative lower cost combined with high levels of integration, or transistor packing densities (# of transistors / silicon area). Bipolar transistor process is more prone to defect density than a process using only majority carrier devices [Gil98]. Therefore, CMOS process will always have higher yield which contributes to lower cost per die. On top of that, as mentioned earlier, pure bipolar processes are rarely seen these days due to its low integration level. Bipolar transistors are often realized in a BiCMOS process which requires more masks, consequently, added cost.

However, if we listen to the other side of the story, the one presented by Bipolar fans, the cost advantage of CMOS process may not be that big. One argument is that [Gil98], many RF or analog chips are quite small, by the time costs associated with package and testing are included, the price tag on the RF chips are not too different. And if we include all the digital chips in a wireless system, the cost advantage of RF CMOS may not be realized at all in a wireless chipset. There is more: an RF or analog CMOS process is different compared to its pure digital counterpart. It requires more masks in order to deliver good quality passive components like resistors, capacitors and inductors. Therefore the CMOS cost advantage associated with masks may be hard to realize. On top of that, bipolar transistors match better than MOSFETs; its performance advantages (for example low 1/f noise) may help to integrate more circuits (for example VCO) on chip or realize lower cost architecture (like direct conversion radio). All these seem to support Bipolar

fans' claim: there is no significantly distinctive cost advantage of CMOS process over Bipolar or BiCMOS.

We believe RF CMOS does pose a cost advantage over BiCMOS for same lithography node technologies. However, this cost advantage may not be fully realized unless for the case of Radio or System on Chip (RoC or SoC) where wafer cost is a large portion of the total system cost; or, for the case where RF transceiver can be designed in a purely low cost digital CMOS process where additional masks related to high quality passive components are not needed. A more comprehensive discussion on the scenarios where RF CMOS will have distinctive advantages is presented in section 2.4.4.

2.4.3 Performance Advantages

There is no doubt that bipolar transistors offer a lot of performance advantages over MOSFETs in RF and analog applications. To name a few here:

1. large g_m/I ratio that is important to specifications like gain and power consumption; (g_m/I of MOSFET will never exceed that of a bipolar transistor [Abo00].)
2. BJT's have lower $1/f$ noise than MOSFET's; low $1/f$ noise is critical in oscillator design and low jitter applications;
3. Bipolar transistors have better device matching on the same die. This is directly related to I/Q match, hence the quality of the radio system;
4. Bipolar transistors have analog characteristics that are accurate thus highly predictable [Gil98] and easily modeled, compared to hard-to-model deep sub-micron CMOS transistor behaviors. Modern BJT devices have model parameters less than thirty while deep sub-micron CMOS devices have model parameters exceed hundreds and every MOS

geometry requires a different model. Even with that, RF CMOS modeling is still not accurate in predicting impedance and noise figure;

5. Bipolar transistors can be biased at relatively large voltage than MOSFET's without reliability concern due to hot carrier degradation [Liq01]. For RF bipolar transistors, the collector-emitter voltage V_{ce} can be as high as V_{cc} . While for deep sub-micron MOSFET's, the drain-source voltage V_{ds} may have to be biased substantially below V_{DD} for analog application. The device lifetime of a $0.18\text{ }\mu\text{m}$ gate length MOSFET biased in saturation at $V_{ds} = V_{DD}$ will be much less than 10 years. The same V_{DD} can guarantee 10 year lifetime for digital circuits because the transistors act as digital switches. They only stay in saturation when the switches are in transition, which is a small portion of the clock cycle. RF or analog CMOS circuits may be forced to operate at a lower power supply voltage, consequently provide less head-room or leg-room compared to bipolar circuits.

However, bipolar transistors are not superior to MOSFET's in every aspect. There are a few interesting performance advantages that CMOS transistors possess. One of them is linearity [Gil98]. (The linearity of SiGe BJT's is better than Si BJT's.) The exponential I-V law is detrimental to transistors in low distortion, medium/large signal applications. This is especially important in mixer design where signals have been amplified by the preceding LNA, and the linearity requirement is stringent. As demonstrated in Chapter 3, large emitter degeneration is employed in bipolar transistors to achieve high IP_3 . Besides decreasing the gain, inductive degeneration requires large silicon area while resistive degeneration, although it occupies a smaller area, adds extra noise and reduces leg-room. The other advantage of CMOS is a complementary pMOS device. Its RF/IF implementa-

tions have not been explored at all. So, put aside all the argument about cost advantage, CMOS still possess a few, if not many, performance edges over a pure bipolar technology.

2.4.4 RF CMOS Scenarios

After all the discussions and arguments, the future of “RF CMOS” still lies in whether it can deliver cheaper commercial RF chips, or to put it simple, when and where can RF CMOS chips have a significant advantage over Bipolar or BiCMOS ones? Will it ever?

The answer is, of course, “yes!”, but not in every wireless application. There are scenarios where it would be beneficial to implement the radio in CMOS, and there are scenarios where it would be prudent to stay with Bipolar/BiCMOS. For example, when the integration level becomes high enough in some wireless system that “Radio (or System) on Chip” (RoC) is desirable, a chipset may in fact be just one big chip plus a few off-chip components or small supporting chips, then, the die cost of that chip will be a large portion of the whole system cost. A 30% reduction on wafer cost may translate into 15% saving in the overall Bill of Materials (BOM), which will give a significant edge to CMOS chip vendors. Other scenarios may include some (low end) radio systems where both CMOS and BiCMOS are more than adequate, which leads to the “golden rule” of RF CMOS scenarios: if CMOS can do it, there is no need for BiCMOS.

It is the goal of this Ph.D. research to find out whether we can design a CMOS transceiver that is functionally equivalent to a commercial SiGe BiCMOS transceiver used in an IEEE 802.11b high rate Wireless LAN chipset [Pav00]. The CMOS transceiver will be housed in the same package, measured on the same PC board as that of the SiGe transceiver. Thus, the project will provide a unique opportunity to make a more controlled com-

parison of the capabilities of CMOS and SiGe BiCMOS technologies for wireless LAN transceiver applications. In addition, the performance advantages and disadvantages of each technology will be analyzed in detail using different RF building blocks and their impact on RF system performance is investigated. The results presented in this dissertation should provide guidance in identifying situations or scenarios where using “RF CMOS” is an advantage, and help IC companies select the right technology for product development.

CHAPTER 3 CMOS AND SIGE RF RECEIVER BUILDING BLOCKS

3.1 PRISM II System Overview

The IEEE 802.11b high data rate WLAN has been implemented with the Intersil PRISM (Personal Radio using ISM bands) chipset [Pav00]. The benchmark product studied here is the PRISM II.5 (or PRISM II) chipset. A concept diagram is shown below.

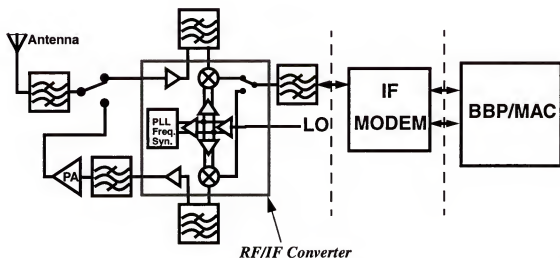


Figure 3-1 PRISM II system concept diagram

The PRISM II WLAN chipset provides a complete solution from antenna to computer for 11 Mbps WLAN systems. The chipset comprises five IC's, 2.4 GHz RF/IF Converter and Synthesizer (RF/IF Converter), 2.4 GHz Power Amplifier with Detector (PA), I/Q MODEM and Synthesizer (IF MODEM), Baseband Processor with Rake Receiver (BBP) and Medium Access Controller (MAC). (The analog front end is identical for

PRISM II and PRISM II.5. The difference is PRISM II.5 integrates the BBP and MAC, 2 separate IC's in PRISM II chipset, into one IC, reducing the IC counts to four.)

The system employs a traditional superheterodyne architecture. On the receiver side, the antenna is routed to a ceramic band pass filter (BPF) which attenuates out of band signals as well as the 1.7 GHz image signals. The received signal then goes to the RF/IF chip which converts the signal at an RF frequency of 2.400 to 2.484 GHz (ISM band) to an IF frequency of 374 MHz. An RF synthesizer is included in the IC with an off-chip VCO. On the transmitter side, the same RF/IF chip converts the signal at 374MHz to an RF frequency in the ISM band. A PA then boosts the signal to around 17 dBm. The outgoing signal after the PA goes through a T/R switch, BPF and antenna diversity switch, and finally reaches the antenna.

A differential 374 MHz SAW filter with 8 dB loss follows the RF/IF converter. The main function of this SAW filter is channel selection. The IF chip converts the received signal after SAW to baseband (receiver) or modulates the baseband transmit signal to IF (transmitter). The BBP implements the IEEE 802.11 CCK modulation while the MAC serves as a digital interface between the 11 Mbps data and computer/controller.

The RF/IF converter is the focus of this dissertation. It is a half duplex transceiver realized in a SiGe BiCMOS process with a peak npn f_T of 50 GHz. The receiver chain features a low noise amplifier (LNA), followed by a down conversion mixer. The output of LNA is not connected to the Rx mixer input directly on-chip. The RF output signal from LNA goes off-chip first and then back on-chip to the Rx mixer input. This provides flexibility of system design since an off-chip Image Rejection Filter (IRF) can be placed here to boost the image rejection if necessary. The IRF can be a ceramic filter or a simple LC

low pass filter or notch filter depending on kinds of image rejection required. In PRISM II, the IF frequency is chosen such that the image frequency falls into a quiet band. The BPF after the antenna provides 45 dB rejection at the image frequency. The narrow band response of LNA and Rx mixer delivers additional 15 dB image rejection. The combined 60 dB image rejection will be able to knock down the jammer at the image frequency most of the time. Based on the system requirement, a designer can choose a simple low cost LC filter or choose not to use an IRF at all.

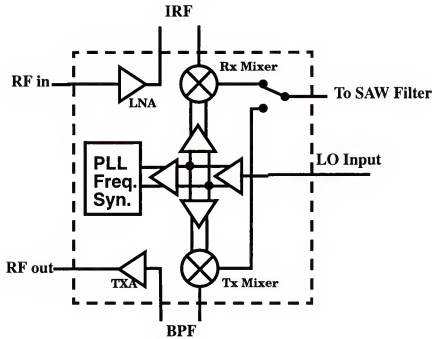


Figure 3-2 Transceiver (RF/IF converter) chip components

The transmit (Tx) chain consists of an up conversion mixer and a transmit amplifier (TXA). Again, the output of Tx mixer goes off-chip, then back on-chip to TXA input. A BPF may be placed after Tx mixer, prior to TXA, to attenuate various spurious components like LO, image, and their harmonics, out of the Tx mixer output. Alternatively, if the

TXA output goes to another BPF before PA, the BPF preceding TXA can be omitted, which is the case in PRISM II.

The remaining circuitry of the RF/IF converter comprises an RF Phase Lock Loop (PLL) frequency synthesizer. Since the VCO is off-chip and usually LO input is single ended, on-chip LO buffers are designed to convert and deliver the differential LO signals to Rx mixer, Tx mixer and prescaler, respectively.

3.2 Low Noise Amplifier (LNA)

3.2.1 LNA Introduction

Low Noise Amplifier (LNA) usually serves as the first active stage of the receiver chain. Its high gain and relative low noise help to lower the overall noise figure of the receiver by reducing the impact of noise from subsequent stages [Poz01].

3.2.2 CMOS and SiGe LNA Design

Fig. 3-3 shows the schematic of a CMOS LNA.

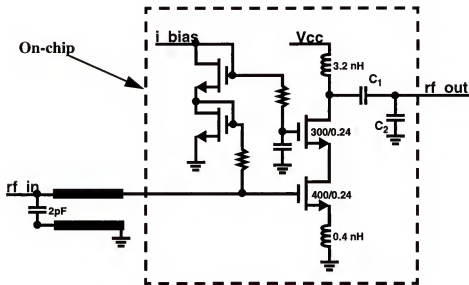


Figure 3-3 CMOS LNA schematic

The SiGe LNA has a similar schematic with a slightly different output matching network as shown in Fig. 3-4.

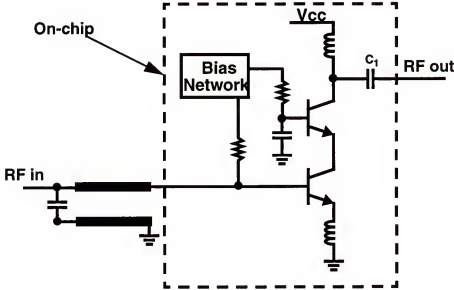


Figure 3-4 SiGe LNA concept schematic

Both CMOS and SiGe LNA's are single stage cascode amplifiers with inductive degeneration, a topology widely used and successfully implemented [Ho00, Flo01]. Compared to common gate or common source, this topology provides better isolation and reduced Miller effect. Single stage also helps to maintain good linearity and low power consumption. Both LNA's have input and output matched to $50\ \Omega$. For the output matching networks, the SiGe one uses an L matching network, i.e., C_2 is absent, while the CMOS one uses a π matching network. The reason for this is, in a digital CMOS process, C_1 is implemented using a poly-to-n-well capacitor [Hun98]. The poly-to-n-well capacitor has significant parasitic capacitance from its bottom plate. This makes the π matching network inevitable [Ho00]. On the other hand, in the SiGe BiCMOS process, an MIM capacitor with small parasitic capacitance is available and a simple L matching network can be eas-

ily implemented. The π matching network brings an extra degree of freedom in matching therefore eases the design of output matching network. It also allows higher Q than that of an L matching network.

As the first step of this research project, (before building the entire CMOS transceiver), a stand-alone CMOS LNA was built and its silicon measurement results were compared to those of the SiGe LNA, which is a part of the SiGe transceiver chip. Both circuits are housed in a 44 pin Micro Lead Frame (MLF) package with an exposed paddle. Fig. 3-5 shows a micro-photograph of the stand-alone CMOS LNA, it is $1100\text{ }\mu\text{m} \times 1000\text{ }\mu\text{m}$. The active areas of the two LNA's are very close and both are pad limited. The pads of the CMOS LNA have the same size and similar spacing as those of the SiGe LNA. The pad arrangement, function and orientation are also the same, so they can be bonded up in the same 44 pin MLF package with the same pinout.

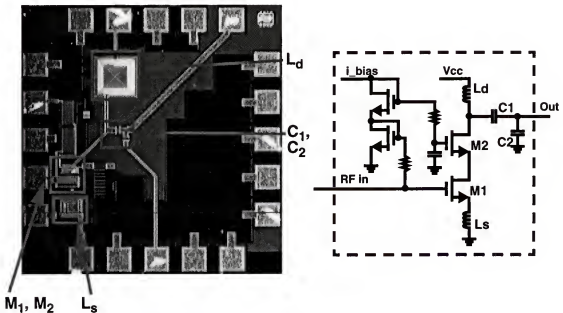


Figure 3-5 A micro-photograph of the CMOS LNA

3.2.3 CMOS LNA Performance

The CMOS LNA was tested on the same PC board designed for the SiGe transceiver. Table 3-1 lists the measured results of CMOS and SiGe LNA's. Most of the CMOS specs are close to or exceed those of the SiGe ones, and this is achieved at the cost of an additional 1.1 mA, or roughly 15% increase in bias current. The bias current of CMOS LNA was chosen to match the SiGe LNA performance.

Table 3-1 CMOS and SiGe LNA Performance Comparison

$f_0 = 2.45 \text{ GHz}$	CMOS LNA	SiGe LNA
50- Ω NF	2.88 dB	2.86 dB
Bias Current	8.1 mA	7.0 mA
Transducer Gain	15.1 dB	15.9 dB
S_{11}	-14.2 dB	-12.7 dB
S_{22}	-20.2 dB	-16.0 dB
S_{12}	< -34	< -30
IIP ₃	2.2 dBm	-2.6 dBm
IP _{1dB}	-7.0 dBm	-11.2 dBm

Fig. 3-6 shows the measured CMOS LNA S-parameters and noise figure. Fig. 3-7 shows the measured CMOS LNA P_{out} versus P_{in} plots. The IIP₃ and IP_{1dB} of CMOS LNA are 4.8 dB and 4.2 dB higher than those for the SiGe one. This is expected since MOSFET's are generally more linear than BJT's under the similar bias condition. Lastly, the circuit can also be made to operate at the same supply current as the SiGe one. This will result in a 0.05 dB increase in noise figure and 0.5 dB decrease in gain, which are small differences.

The overall performance of the stand-alone CMOS LNA matches the SiGe one's with a slight increase in power consumption. This design will be ported into the CMOS transceiver with no major changes when the full chip CMOS transceiver is realized.

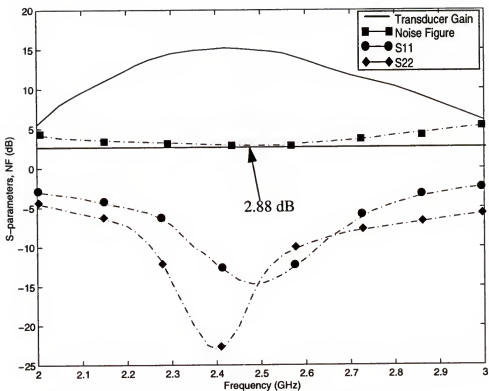


Figure 3-6 Measured CMOS LNA S-parameters and Noise Figure

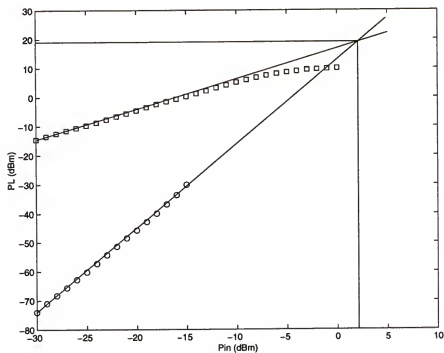


Figure 3-7 The output 1dB compression point and IP3 measurement for the CMOS LNA

3.2.4 Comparison of CMOS and SiGe LNA's

The CMOS LNA was designed to meet the specifications of the SiGe LNA and measurement results seem to agree with simulations. It certainly merits some analytical discussion. Here we would like to present a brief analysis and explanation. A more detailed discussion will be presented in chapter 5.

From the small signal ac model of cascode LNA's shown in Fig. 3-8, for both CMOS and SiGe bipolar LNA's, the input impedance can be expressed approximately as [Okk02, Flo01, Sha97]:

$$Z_{in} = j\omega(L_{in} + L_{deg}) + \frac{1}{j\omega C_{in}} + \frac{g_m}{C_{in}} L_{deg} + r_{in} , \quad (3.1)$$

where L_{in} represents L_B or L_g , and L_{deg} represents the degeneration inductor L_e or L_s , C_{in} represents input capacitance C_π or C_{gs} , and g_m is the transconductance of the input transistor. r_{in} is gate (r_g) or base (r_b) resistance. For LNA, it is usually small (for low noise purpose) and will be neglected in the following analysis. (The exact solution of the input impedance and various approximations are presented in Appendix B.) Z_{in} takes the form of a series RLC resonant network, with resonant frequency

$$f_0 = \frac{1}{2\pi \cdot \sqrt{(L_{in} + L_{deg})C_{in}}} . \quad (3.2)$$

At resonance, the input impedance is purely resistive:

$$Z_{in} = \frac{g_m}{C_{in}} L_{deg} \sim 2\pi f_T L_{deg} , \quad (3.3)$$

where f_T is the unity transit frequency of the transistor and the quality factor of this network including source resistance Z_0 is,

$$Q_{in} = \frac{1}{2\pi f_o C_{in} \cdot (Z_0 + 2\pi f_T L_{deg})} \sim \frac{1}{4\pi f_0 C_{in}} \quad (3.4)$$

The effective G_m of the tuned RLC resonant network is:

$$G_m \sim Q_{in} \cdot g_m \quad (3.5)$$

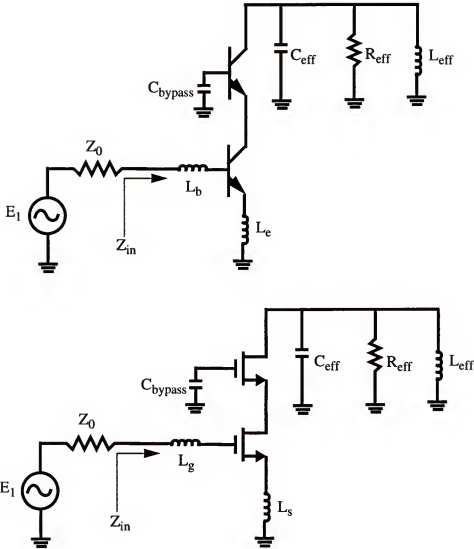


Figure 3-8 Small signal model of cascode LNA's

The g_m/I ratio of CMOS is lower than that of bipolar [Abo00]. The dc currents of two LNA's are close; therefore, the g_m of CMOS LNA input transistor is lower than the

SiGe LNA's. However, SiGe LNA adopted a Q_{in} lower than the CMOS one, resulting in a similar overall effective G_m for both LNA's. (The reason why BJT LNA has a lower Q_{in} will be discussed in chapter 4.)

Effective G_m and the load seen at the cascode collector/drain R_{eff} , determine the overall power gain:

$$G_T \sim G_m^2 \cdot R_{eff} \cdot R_s \quad . \quad (3.6)$$

Both LNA's have similar R_{eff} , therefore their power gains are close. The analysis brings up a general question: how do we deal with low g_m/I of CMOS as g_m/I of MOSFET will never reach that of a bipolar transistor? Generally there are three things we can do, first, consuming more current; second, utilizing a larger load (At high frequencies, an inductive load is more often used than a resistive load, increasing the load is equivalent to increasing the Q of the inductor when the inductance is fixed); third, increasing the Q of tuned circuit; by carefully balancing these three things, CMOS can match SiGe RF amplifier performance with a small increase in power consumption. Furthermore, as technology advances, g_m/I of MOSFET will increase [Abo00]. Operating the device near weak inversion will also help to reduce power consumption. All these point to a promising future of CMOS implementation of LNA's or RF amplifiers.

3.3 Receive Mixer

3.3.1 Receive Mixer Introduction

Mixer is another important block in the receiver chain. Its main function is to achieve frequency conversion. In a superheterodyne receiver, the Receive (Rx) mixer down converts the signal at RF frequency to IF frequency. Since it is placed after the LNA which has a gain around 15 to 20 dB, mixer usually requires a high linearity. An active

mixer achieves the frequency conversion as well as provides gain, therefore it helps to maintain the high gain and low noise figure of the overall receiver. A popular IC implementation of the active mixer is a Gilbert mixer.

3.3.2 CMOS and SiGe Rx Mixer Design

Fig. 3-9 shows the schematic of CMOS and SiGe Rx mixer cores. The mixer is a Gilbert type double balanced active mixer. Two mixers have the identical schematic, except for the fact that all the nMOS transistors in the CMOS mixer are replaced by npn BJT's in the SiGe mixer.

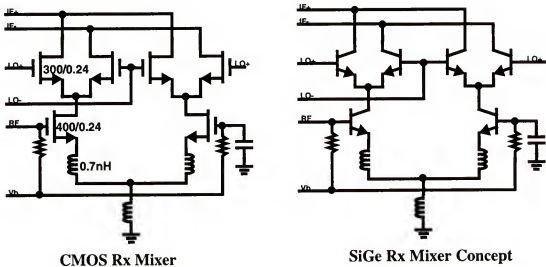


Figure 3-9 CMOS and SiGe Rx mixers schematic

For both mixers, the RF input is matched to $50\ \Omega$ using similar matching network used for the LNA input matching. The IF outputs are matched to a $200\text{-}\Omega$ differential load through an off-chip matching network shown in Fig. 3-10. The inductor and capacitor values for the output network are the same for CMOS and SiGe mixers while the resistive loads are different. The CMOS mixer uses $2.5\text{ k}\Omega$ resistor, more than twice the value used in the SiGe mixer. A larger load in CMOS helps to compensate its relatively lower g_m so

that both mixers exhibit similar conversion gain. The $200\ \Omega$ differential load represents the SAW filter at 374 MHz. It is only resistive at IF frequency.

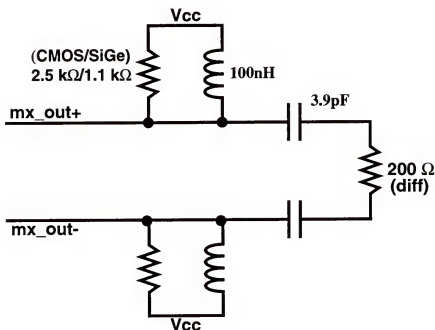


Figure 3-10 Rx mixer output matching network

3.3.3 LO Converter and Buffer

As mentioned, in the PRISM II system, Local Oscillator (LO) signal is generated by an off-chip VCO. The LO input signal coming into the transceiver chip is single ended. The LO differential signal is generated on chip through the LO buffer circuitry. The single-ended output of the off-chip VCO is converted to differential using an on-chip converter. This differential signal is then buffered through source followers and amplified to drive the mixer switching core in the Rx mixer case. The Rx mixer, Tx mixer and prescaler share one LO single end to differential converter, followed by their buffers, as illustrated in Fig.3-11.

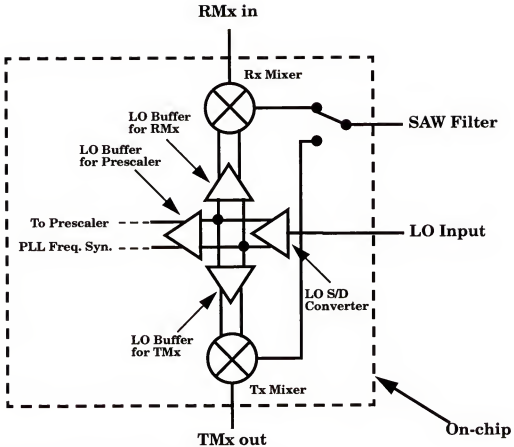


Figure 3-11 LO Converter/Buffer concept diagram

Fig. 3-12 shows the CMOS converter/buffer schematic. The circuit implementations of the SiGe counterparts are similar. The only difference is the load of the driver (amplifier). In the SiGe chip a resistive load is used while in the CMOS case an inductive load is employed to deliver a larger LO swing. As explained in section 3.3.4, a large LO swing is important for CMOS mixer performance. The inductive load renders a narrower band response in contrast to the wide band response for a circuit with a resistive load. This however, will not pose a problem, since for a given radio, the IF frequency is fixed in the superheterodyne architecture, and the system bandwidth is only 83 MHz in PRISM II.

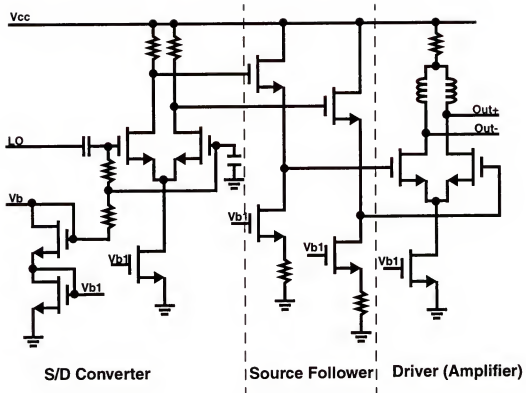


Figure 3-12 CMOS LO Buffer Schematic

3.3.4 Comparison of CMOS and SiGe Rx Mixers

Similar to the LNA case, as the first step of this research project, (before building the entire CMOS transceiver), a stand-alone CMOS Rx mixer was built and its silicon measurement results were compared to those of the SiGe Rx mixer, which is a part of the SiGe transceiver chip. The reason to build stand-alone CMOS LNA and Rx mixer is, the receiver component specifications are usually more stringent and challenging. By building stand-alone circuits and comparing its hardware results with the SiGe transceiver chip, we are able to assess the feasibility and difficulty of the project. Consequently this allowed more reliable estimation of the amount of the work and realistic planning of the entire chip.

Fig. 3-13 shows a micro-photograph of the CMOS mixer. The die size of the CMOS mixer is $1500\text{ }\mu\text{m} \times 1100\text{ }\mu\text{m}$.

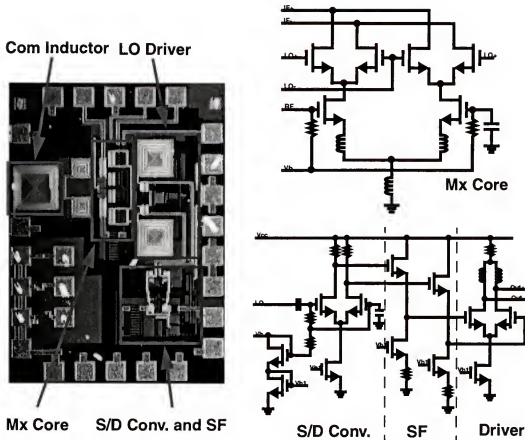


Figure 3-13 A micro-photograph of the CMOS Rx mixer.

Table 3-2 lists the measurement results of the two mixers. The CMOS mixer exhibits approximately the same gain and return losses. The SSB noise figure is 1.5 dB higher for the CMOS mixer. An explanation for this is, for the CMOS mixer, with sinusoidal LO signals, the switching core transistors are simultaneously on for a larger portion of a period than its SiGe bipolar counterpart. Even though for the CMOS mixer, the LO signal is designed to have twice the magnitude as that of the bipolar one, namely, 0.3 V versus 0.15 V, the amount of time when both switching transistors are on is still larger than that in

the bipolar differential pair switches. Additionally, the CMOS LO buffer chain consumes a total 8 mA current, of which, 3 mA is for the single-end to differential converter, 1 mA is for the source follower and 4 mA is for the driver. On the other hand, the SiGe LO buffer chain consumes only 5 mA, of which, 2 mA is for the single end to differential converter, 1mA is for the emitter follower and 2 mA is for the driver. A large LO swing at the mixer switching core is critical to CMOS mixer performance (for both the conversion gain and noise figure). This is a reason that the bias current of the CMOS buffer chain is higher and its LO driver utilizes an inductive load while its SiGe counterpart consumes lower current and employs a resistive load.

Table 3-2 CMOS and SiGe Rx Mixer Comparison

LO=2.1GHz	CMOS Mixer	SiGe Mixer
Power Gain	8.0 dB	8.1 dB
SSB NF	10.5 dB	9.0 dB
Core Bias Current	12 mA	10 mA
LO Buffer Bias	8 mA	5 mA
RF Input S_{11}	-12.4 dB	-20.5 dB
LO Input S_{11}	-12.3 dB	-10.7 dB
IF Output S_{11}	-11.6 dB	-15.0 dB
IIP_3	3.0 dBm	6.2 dBm
IP_{1dB}	-6 dBm	-3.1 dBm
LO to IF feedthru	-32 dB	-40 dB

Fig. 3-14 plots the measured curves for extracting IP_3 and P_{1dB} of the CMOS mixer. Contrary to the LNA case, IIP_3 and IP_{1dB} of the SiGe mixer are 3 dB better than that of the CMOS one. There are two reasons for this. First, in the SiGe mixer, the inductive degeneration for the RF transistors (M1 & M2) is 2 nH, which is much higher than 0.7 nH used in the CMOS mixer. This inductor was kept lower to achieve the same gain in CMOS mixer without increasing the power consumption. Second, the larger LO signal for

the CMOS mixer introduces a larger signal at twice the LO frequency (2-LO signal) on the drain node of the RF transistors. This 2-LO signal is coupled to the gates of RF transistors through C_{gd} of the MOS transistors and is known to degrade the linearity performance. Despite the slightly inferior noise figure and IIP_3 , the CMOS mixer still satisfies the Rx mixer specifications for the PRISM II system.

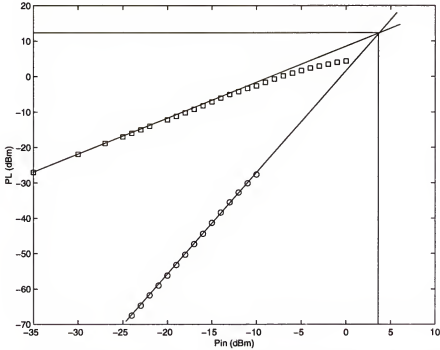


Figure 3-14 The output 1dB compression point and IP3 measurement for CMOS Rx Mixer

3.3.5 Summary of Rx Mixer Design

The stand-alone CMOS Rx mixer exhibits similar performance as its SiGe bipolar counterpart. This CMOS Rx mixer design will be ported into the CMOS transceiver chip with no major changes. One adjustment will be made from a system point of view: the common mode inductor will be replaced by a current source. The reason is that, this common mode inductor tends to pick up low frequency noise and spurs from the substrate due

to its relative large area. (It's a large inductor, shown in Fig. 3-13.) This adjustment shows little impact on mixer performance in simulation.

CHAPTER 4

Q OF RF TUNED CIRCUITS IN DIFFERENT IC TECHNOLOGIES

4.1 The Impact of Q

From the LNA design analysis, we can see the importance of Q of the tuned circuit. The tuned matching networks are desired in RF circuits because they reject out of band unwanted signals and consume less power compared to broadband amplifiers [Okk02]. However, the Q of the matching network can not be arbitrarily large, especially for integrated circuits. IC manufacturing exhibits significant process variations from lot to lot, wafer to wafer, and die to die. On top of that, variations due to temperature, supply voltage, packaging, PC board environment, etc. will all affect RF circuit performance. Therefore, the Q of the RF circuits should be sufficiently low to withstand these variations. A proper selection of Q value is a key for circuit yield and system integrity.

4.1.1 Q of Simple Second Order System

Typically, matching networks can be modeled as second order systems with a transfer function as [Okk02]:

$$H(j\omega) = \frac{1}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)} \quad (4.1)$$

A radio system is usually designed to work in a certain frequency range. The overall frequency response of the amplifiers in a radio is required to be flat in that frequency

range. Usually, it is specified as ± 0.5 dB over a certain frequency range ($\Delta\omega$). Gain flatness of ± 0.5 dB over $\Delta\omega$ is the 1-dB band width requirement, as illustrated in Fig. 4-1.

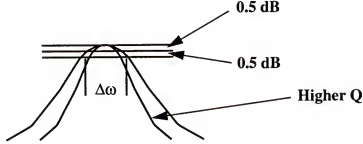


Figure 4-1 Frequency response and Q of the network

4.1.2 The Impact of Q on Tuned RF Circuit Design

Let's assume power gain is approximately proportional to $|H_{in}(j\omega)|^2 |H_{out}(j\omega)|^2$ in an LNA. Furthermore, for simplicity, let $|H_{in}(j\omega)| = |H_{out}(j\omega)|$, and assume all the frequency response of the circuit comes from these two terms. To satisfy the gain flatness,

$$10 \log \left| H \left(j \left(\omega_O + \frac{\Delta\omega}{2} \right) \right) \right|^4 = -1 \text{ dB} , \quad (4.2)$$

or,

$$\left| H \left(j \left(\omega_O + \frac{\Delta\omega}{2} \right) \right) \right| = 10^{-\frac{1}{40}} = k . \quad (4.3)$$

Since $\Delta\omega/2$ is set for a system, the only unknown is Q. Solving for Q,

$$Q = \sqrt{\frac{\frac{1}{k^2} - 1}{\left(\frac{\omega_O + \frac{\Delta\omega}{2}}{\omega_O} - \frac{\omega_O}{\omega_O + \frac{\Delta\omega}{2}} \right)^2}} . \quad (4.4)$$

The gain flatness sets the Q for the input and output matching networks. Q can not be arbitrarily high. From the CMOS and SiGe BJT LNA comparison discussion in chapter 3, increasing Q or increasing current can help to increase the overall G_m , consequently increase gain. So, higher Q is beneficial to lower power consumption, and there is a trade-off between power consumption and bandwidth of a receiver. On the other hand, a circuit with high Q networks is more sensitive to component variations [Flo01, Okk02]. This is a serious issue in IC implementation, where process variation typically renders more than 10% change of passive component values.

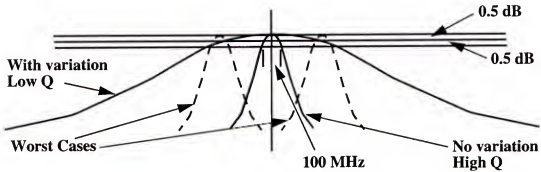


Figure 4-2 Component variation and Q

For example, in a 802.11b radio system, if the LNA is required to have gain flatness of ± 0.5 dB from 2.4 GHz to 2.5 GHz, without any component variations, from Eq. (4.4) Q should be less than 8.5. Now, suppose the components which determine the tuning characteristics (i.e. L and C) are controlled within $\pm 10\%$. If the LNA is centered at 2.45 GHz, in the worst case the tuned frequency could be as high as 2.695 GHz (110% of 2.45 GHz) or as low as 2.205 GHz (90% of 2.45 GHz). To make sure that even in the worst case, the design satisfies the gain flatness requirement, it must have an 1-dB bandwidth of

$2 \times (2.45 \text{ GHz} \times 10\% + (2.5 \text{ GHz} - 2.4 \text{ GHz})/2) = 590 \text{ MHz}$ as illustrated in Fig. 4-2. Plugging 590 MHz back into Eq. (4.4) as $\Delta\omega$, we find out that Q should be less than 1.5.

4.2 Q and Different IC Technologies

If the Q of a network is too high that the component variations affect the circuit performance more, then the overall wafer yield will become lower. In the LNA comparison discussion, we found out that CMOS LNA has a higher input Q than that of the SiGe BJT LNA. A logical question from there is that, is it because BJT devices have more process variations that they have to be designed with a lower Q, or is it because in order for CMOS technology to match the performance of SiGe BJT under similar bias condition, the Q of the input network has to be higher? The different circuit Q values for different technologies have to be justified: lower Q of BJT circuits may render the advantage of higher g_m/I ratio of bipolar transistor useless; on the other hand, higher Q of CMOS circuits may undermine the very nature of choosing RF CMOS if the high Q lowers the circuit yield and raises the cost.

If the resistance value is fixed in the RLC resonant circuit, (like in the case of LNA input matching where the resistance is fixed at 50Ω), for a series resonant circuit, lower capacitance or higher inductance implies higher Q; for a parallel resonant circuit, lower capacitance or higher inductance means lower Q.

Before we get into the discussion of which technology will have more process variations or enable use of higher Q circuits, let's first examine which technology will likely to have lower capacitances so we know for series or parallel circuits which technology will more likely to have a higher Q design.

4.2.1 BJT and MOS Capacitances

Which technology will more likely to have a small capacitance, BJT or MOS technology? The answer is MOSFET. This can be demonstrated by looking at one of the key figures of merit of CMOS and bipolar technologies, the unity gain frequency f_T which can be expressed as [Gra93],

$$f_T \equiv \frac{1}{2\pi} \cdot \frac{g_m}{C_T} \quad (4.5)$$

where C_T is $C_\pi + C_\mu \sim C_\pi$ in BJT's and $C_{gs} + C_{gd} \sim C_{gs}$ in MOSFET's; g_m is the transconductance and in a bipolar transistor, it is always,

$$g_m = \frac{I_c}{V_T} \text{ or } \frac{g_m}{I_c} = \frac{1}{V_T} = \frac{q}{kT} \sim 0.038 \text{ V}^{-1} \quad (4.6)$$

at room temperature. While in a long channel MOSFET, g_m is,

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \text{ or } \frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{th}} \quad (4.7)$$

The g_m/I ratio of a MOSFET (4.7) is always smaller than and will never exceed that of a BJT (4.6) [Abo00]. Therefore, Eq. (4.5) indicates that, for an nMOS and an npn BJT exhibiting the same speed (f_T), if they are biased under the same current, MOSFET will have a smaller g_m consequently smaller capacitance, i.e., it is more likely to have $C_{gs} < C_\pi$. This is further illustrated in table 4-1. Two devices exhibiting the same f_T are picked from two technologies. In CMOS technologies, a high f_T is achieved through a smaller C_{gs} , while in bipolar technologies the same f_T is obtained through a higher g_m [Man01].

Table 4-1 Characteristics of an nMOS and a bipolar npn

Parameters	0.18 μm CMOS	Parameter	0.3 μm Si BJT
C_{gs}	92 fF	C_{π}	230 fF
f_T	43 GHz	f_T	43 GHz
g_m	30 mA/V	g_m	100 mA/V
I_{DS}/W	$\sim 50 \mu\text{A}/\mu\text{m}$	I_C/L_E	$\sim 80 \mu\text{A}/\mu\text{m}$
Width W	$\sim 70 \mu\text{m}$	Emitter width L_E	$\sim 30 \mu\text{m}$

4.2.2 Series Resonant Circuits

Since MOSFET's are more likely to have smaller capacitance, for series resonant circuits like the LNA input, CMOS circuits are more prone to higher Q design, a potential hidden performance disadvantage that can not be seen in chapter 3 until the details of the actual circuits are revealed here. Extra care should be taken in RF CMOS series resonant circuit design to ensure proper selection of Q value.

Let's look at the example of our LNA input matching. Rewriting Eq. (3.3) of Z_{in} , the input impedance of LNA is,

$$Z_{in} = \frac{g_m}{C_{in}} L_{deg} \sim 2\pi f_T L_{deg} \quad (4.8)$$

In both BJT and MOS LNA's, Z_{in} should be matched to $(50 \Omega - r_g \text{ or } r_b)$. (r_g or r_b is small for well-designed LNA therefore they can be neglected.) We realize that L_{deg} is the same in the CMOS and bipolar LNA design ($L_s, L_e \sim 0.4 \text{ nH}$), therefore CMOS and SiGe BJT LNA should have the same f_T . Since both LNA's are biased under similar current, g_m of CMOS will be lower than that of SiGe BJT. Consequently, the input capacitance C_{in} of CMOS LNA is smaller; hence, CMOS LNA exhibits higher Q and is potentially more sensitive to component variations.

A detailed analysis on MOS LNA Q and input matching can be found in [Flo01].

There, an alternative input quality factor independent of L_s is defined as

$$Q_{gs} = \frac{1}{\omega_o C_{gs} Z_0} . \quad (4.9)$$

Assuming in Eq. (3.1), inductors, C_{in} and f_T all have tolerance of 10%, to satisfy input matching $S_{11} < -10$ dB, Q_{gs} should be less than 2.3 [Flo01]. In section 4.1.2, we estimated Q of all the matching networks in LNA should be less than 1.5 to ensure the gain flatness. This is consistent with Q_{gs} estimate here because Q_{gs} is roughly twice the Q of LNA input matching network including the source resistance. It is prudent to recommend a Q_{gs} of no more than 3 for 2.4 GHz LNA input design.

The above analysis indicates that, for the same speed performance, since C_{in} is larger for a BJT series resonant circuit (BJT LNA input), it has lower Q. Does this mean a BJT RF circuit poses an advantage in terms of process variations since its Q is lower? Not necessarily, this is only true if, for the same Q, BJT devices exhibit the same process variations as MOS devices.

4.2.3 Parallel Resonant Circuits

In a parallel resonant RLC circuit, for a fixed parallel resistance, a lower capacitance means lower Q which will give MOSFET circuits some advantage. This usually occurs is the case of multi-stage RF circuitry in Fig.4-3, where the previous stage has an inductor load and the ensuing stage is the input of a transistor. For example, the previous stage could be the LNA and the ensuing stage could be the input of the receive mixer; or, the previous stage could be the first stage of a two-stage amplifier, etc.

If there is no fixed resistor in parallel with the capacitor or inductor, $\frac{1}{Q_{total}} = \frac{1}{Q_L} + \frac{1}{Q_C}$. Therefore, the Q of the resonant LC circuit will follow the smaller one of the Q's of capacitor and the inductor. In an IC environment, it is usually the inductor Q which is smaller. The Q of the parallel resonant tank is determined by the Q of the on-chip inductor. A high Q inductor is not always desired: circuits using such inductors are less tolerant to process variations.

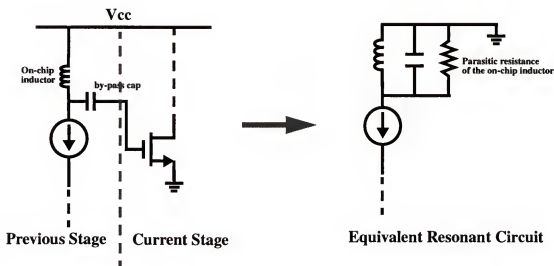


Figure 4-3 Parallel resonant circuit in RF IC's

4.3 Process Variations of IC Technologies

From the analyses in previous sections, we realize that process variations are one of the main reasons to design tuned circuits with low Q. Different technologies may exhibit different levels of process variations. For the same Q, two tuned RLC circuits in BJT and MOSFET may have a different component value shift. The assumption of 10% component value shift is somewhat rough and over-simplified. Detailed assessment of process variations in different technologies should be conducted and is carried out in this sec-

tion. The discussion is restricted to BJT and MOSFET technologies only, since these are the two technologies of interest for WLAN applications. However, the methodology developed here is generic and can be applied to other IC technologies. Variations of two key figures of merits, f_T and C_π (or C_{gs}) for BJT and MOSFET devices are evaluated.

4.3.1 Process Variations of BJT and CMOS Technologies

For a BJT, the peak f_T is proportional to τ_f . For a good BJT device (high emitter efficiency), τ_f is close to base transit time τ_B which is related to base width W_B . Therefore we have

$$\tau_f \cong \frac{W_B^2}{v D_n} \quad (4.10)$$

where D_n is the diffusion constant and v is 2 for constant base doping. v can be much larger than 2 for graded doping where the built-in electric field is large. However, there exists a limit for the smallest τ_f that can be achieved,

$$\tau_{f, min} \cong \frac{W_B}{2v_s} \quad (4.11)$$

where v_s is the saturation velocity of electron. Either way, the control of W_B will determine the variations of f_T and the control of W_B is limited by ion implantation. (For SiGe, W_B variations depend on the thickness control of epitaxial layer deposited using a CVD process). For modern high performance Si or SiGe BJT's, W_B is on the order of 50 nm or less. The control of W_B is a vertical challenge which will not benefit much from the lithography advancement.

For MOSFET's, the variations of peak f_T and C_{gs} are related to W and L which are limited by lithography, and thickness control of the thermal oxidation process. The phys-

ics of process variations behind BJT and MOS transistors are quite different. For SiGe BJT, it's the SiGe epitaxial deposition while for MOS, it is lithography and thermal oxidation. CVD epitaxial layer deposition with a linearly graded Ge profile is likely to have more process variations because it is harder to control compared to thermally grown oxide thickness. Foundry supplied corner model data suggested that the variations of W_B can be around 20% for SiGe BJT's; while only 5% for MOSFET gate oxide thickness. However, for MOSFET, there is also variations associated with the device dimension W and L , termed δL or δW . δL or δW is usually 10% of the lithography resolution, $0.025 \mu\text{m}$ in the case of a $0.25 \mu\text{m}$ CMOS technology. The process variations associated with device dimension ($\delta L/L$ or $\delta W/W$) depends strongly on device size (W and L) because the lithography resolution stays the same for both large and small devices. Devices with larger W and L will exhibit much less process variations (percentage wise, $\delta L/L$ or $\delta W/W$) than devices with smaller W and L . Usually the design rules are set that the minimum W is much larger than the lithography resolution ($0.6 \mu\text{m}$ in $0.25 \mu\text{m}$ CMOS process used). On top of that, MOS devices used for analog or RF applications are usually wide (on the order of tens or hundreds of microns). Therefore, the variation of W , $\delta W/W$ is usually much less than 1%. The variation of L , on the other hand, is one of the main contributors for process variations of RF or analog MOSFET's. Clearly, if MOSFET devices are designed with large gate length, their process variations will be much smaller. For example, MOSFET's with L of $0.5 \mu\text{m}$ exhibit gate length variation of only 5% ($\delta L/L$), compared to 10% of MOSFET's with L of $0.25 \mu\text{m}$. However, large gate length device exhibits slower speed thus not favored for RF circuits.

The scaling down in lithography certainly helps to alleviate MOSFET variations. The vertical device (BJT) does not benefit as much from technology scaling as the lateral device (MOS). All these seem to indicate that MOSFET's can have less process variations than BJT's, especially if the device gate length is larger than the lithography resolution. However, it would be impetuous to jump into the conclusion that BJT devices always have more process variations than MOSFET's. The real comparison should always be process by process, or foundry by foundry.

Figures 4-4 to 4-7 show the simulated MOS and BJT LNA input transistors over process variations. The CMOS process is a 0.25- μm process from a leading CMOS foundry while BJT process is 0.35- μm SiGe BiCMOS process from a leading SiGe BiCMOS foundry. Every stripe of MOSFET device is 100 μm /0.24 μm (gate W/L). Every stripe of BJT device is 10 μm /0.44 μm (emitter length/emitter width). The devices are biased at 7 mA current and are simulated with fast-fast, nominal, slow-slow corner models provided by the foundry. f_T and the capacitance of the input transistors are plotted versus the number of stripes of the unit device. The 7 mA current is close to the current of both BJT and MOS LNA's discussed in chapter 3.

A MOS device and a BJT device providing the same nominal input capacitance around 0.7 pF are picked as input transistors and their dc operating points are simulated under different corner models supplied by the foundries. Results are shown in tables 4-2 and 4-3. For MOS input transistor, f_T and C_{gs} worst case variations are 13% and 3%, respectively; for BJT input transistor, f_T and C_π worst case variations are 27% and 21%, respectively.

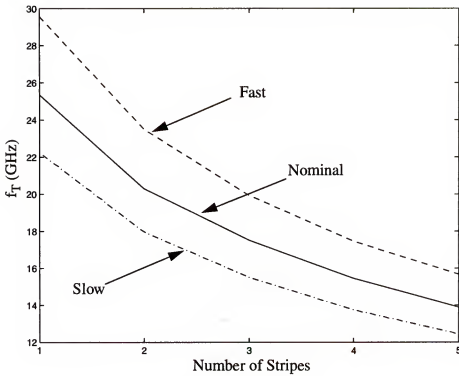


Figure 4-4 MOS LNA input device f_T vs. # of stripes (with process variations), $I_d = 7\text{mA}$.

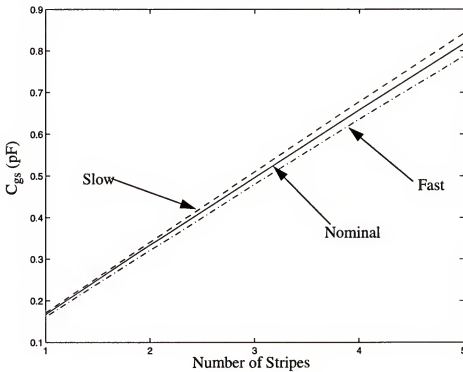


Figure 4-5 MOS LNA input device C_{gs} vs. # of stripes (with process variation), $I_d = 7\text{mA}$.

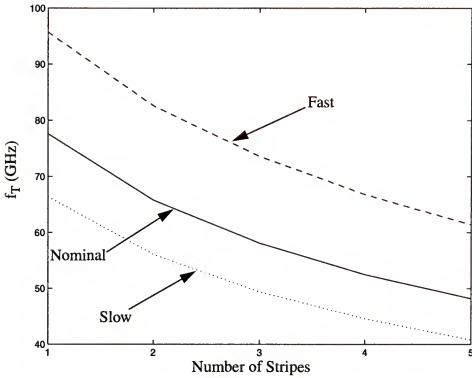


Figure 4-6 BJT LNA input device f_T vs. # of stripes (with process variation), $I_C = 7\text{mA}$.

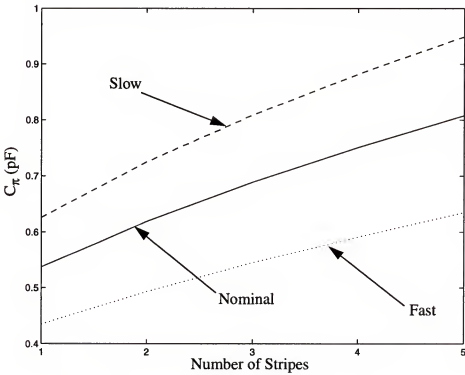


Figure 4-7 BJT LNA input device C_{π} vs. # of stripes (with process variation), $I_C = 7\text{mA}$.

Table 4-2 A $400\mu\text{m}/0.24\mu\text{m}$ nMOS biased at 7mA under different corner models

Parameters	Nominal	Fast	Slow	Worst-case variations
C_{gs} (fF)	658	636	678	3%
g_m (mA/V)	63.9	69.8	58.6	9%
V_{th} (V)	0.503	0.439	0.567	33%
$V_{gs}-V_{th}$ (V)	0.185	0.166	0.203	11%
$f_T \sim g_m/C$ (GHz)	15.5	17.5	13.8	13%

Table 4-3 A $27\mu\text{m}/0.44\mu\text{m}$ npn biased at 7mA under different corner models

Parameters	Nominal	fast	slow	Worst-case variations
C_π (fF)	668	530	790	21%
V_{be} (V)	0.877	0.858	0.904	3%
Intrinsic r_b (Ω)	9	12	6	33%
Extrinsic r_b (Ω)	6	3	9	33%
Total r_b (Ω)	15	15	15	$\sim 0\%$
τ_f (nS)	2.3	1.75	2.8	24%
β	89	235	29	164%
r_π (Ω)	335	883	109	164%
$f_T \sim g_m/C$ (GHz)	64	81	54	27%

It seems that for the two processes in comparison, MOSFET's have less process variations than BJT's. This, however, needs further investigation.

4.3.2 MOS Corner Models for RF tuned circuits

The analysis above certainly bodes well for CMOS technology in terms of matching the CMOS amplifier gain with that of BJT amplifier. Bottom line is: it is the $g_m Q$ that determines the gain, not g_m alone. RF circuits in technology with less variations can be

designed with higher Q , therefore, a better $g_m Q$ product which leads to better gain per current.

It was found out in section 4.3.1, that the 0.25- μm CMOS has less process variations than the 0.35- μm BiCMOS technology in simulations. This claim needs to be further investigated before drawing conclusions. The first thing under the microscope is the corner models of MOSFET's used in the simulation. The corner models supplied by the foundry are based on digital CMOS processes. Two ends of the corners, fast (or best) and slow (or worst) models are distinguished by the current driving capability of the devices. They are termed digital-fast and digital-slow models in the rest of the discussion.

For RF applications, the digital-fast and digital-slow models do not reflect the corner scenarios of RF circuits. RF circuits have tuned response with respect to frequency. Therefore, capacitance and peak f_T rather than current driving capability should be used as the criteria to assess the corner situations of RF circuits.

A new MOSFET modeling scheme that provides correct RF CMOS corner models is proposed here. New corner models based upon the new scheme are called RF-fast and RF-slow models. As we can see in the following section, they are quite different from digital-fast and digital-slow corner models.

4.3.3 RF-fast/slow Models vs. Digital-fast/slow Models

The difference between the new RF corner models and the old digital corner models lies in the representation of two key process parameters, oxide thickness and gate length as shown in table 4-4 where L and T_{ox} are the nominal values of oxide thickness and gate length. Digital-fast model represent the case with the thinnest gate oxide thickness and narrowest gate length. It has the highest current driving capability. Yet it does not

have the highest f_T because the effects of thin gate oxide and narrow gate length on capacitance tend to cancel each other.

Table 4-4 RF corner models vs. Digital corner models

Parameters	RF-fast	RF-slow	Digital-fast	Digital-slow
Oxide thickness	$T_{ox} + \delta T_{ox}$	$T_{ox} - \delta T_{ox}$	$T_{ox} - \delta T_{ox}$	$T_{ox} + \delta T_{ox}$
Gate length	$L - \delta L$	$L + \delta L$	$L - \delta L$	$L + \delta L$
Capacitance	Smallest	Largest		
g_m			Largest	Smallest
$f_T \sim g_m/C$	fastest	slowest		

To further illustrate the difference between two corner models, an example is shown here. At 7mA, a MOS device with a number of stripes of 4 ($400\mu\text{m}/0.24\mu\text{m}$) exhibits nominal Q_{in} around 1. The operating point of this device under different models is tabulated in table 4-5. Capacitances and f_T of different size devices are also simulated with the two models. The results are obvious: using the new corner models, the capacitances and f_T varies much more than predicted by the old corner models. For a nominal input capacitance around 0.7 pF, for MOS input transistor, f_T and C_{gs} worst case variations are 22% and 14%, respectively; they are much larger than 6% and 4% from digital models. However, still less than 27% and 21% of BJT device variations.

Table 4-5 A $400\mu\text{m}/0.24\mu\text{m}$ nMOS biased at 7mA under different corner models

Parameters	Nominal	RF-fast	RF-slow	Digital-fast	Digital-slow
C_{gs} (fF)	658	576	751	636	678
g_m (mA/V)	63.9	68.8	58.9	69.8	58.6
V_{th} (V)	0.503	0.439	0.566	0.439	0.567
$V_{gs} - V_{th}$ (V)	0.185	0.168	0.202	0.166	0.203
$f_T \sim g_m/C$ (GHz)	15.5	19	12.5	17.5	13.8

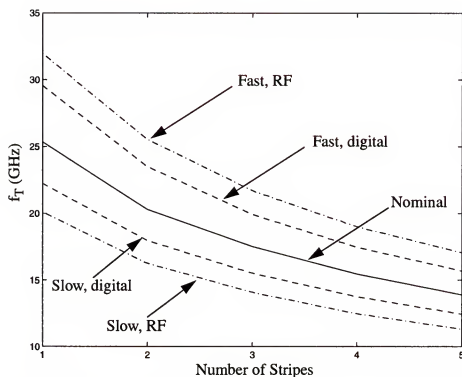


Figure 4-8 MOS LNA Input Device f_T vs. # of Stripes (with Process Variation), $I_d = 7\text{mA}$.

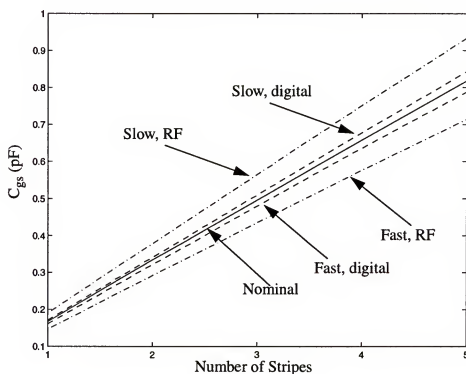


Figure 4-9 MOS LNA Input Device C_{gs} vs. # of Stripes (with Process Variation), $I_d = 7\text{mA}$.

Figures 4-8 and 4-9 show the capacitances and f_T varying as a function of the number of stripes under different corner models. The difference between two corner models is significant. The discussion here points out that the corners supplied by foundry is not modeled from an RF perspective. Often corner models are employed to simulate the worst case scenarios. If the corner situations are not modeled correctly, the circuit may be designed with Q too high or too optimistic. The whole circuit performance and yield will be affected.

4.4 RF Tuned Circuit Under Process Variations.

In order to more fully understand the impact of various variations on circuit performance and the relationship between Q and immunity to variations, process and temperature variations of a simple LNA are simulated with corner model sweep to investigate the circuit level performance.

4.4.1 CMOS and BJT LNA's under Process Variations

The basic LNA circuit in Fig. 4-10 is chosen for this purpose. Input matching of CMOS and BJT LNA's under process variations is compared. Again, the two LNA's are biased at 7 mA dc current. For a fair comparison, the Q of the input matching are set to be the same under nominal condition for two LNA's. A nominal Q of 1 is chosen and this sets the input transistor nominal capacitance (C_{gs} or C_{π}) to be around 0.65 pF at 2.45 GHz. The input is matched under the nominal condition, i.e. the input inductor and the degenerate inductor values are set to match the input port to 50 Ω . The LNA is then simulated under different transistor corner models while maintaining the total current unchanged at 7mA. (For MOS LNA, the newly developed RF corner models are used, replacing the foundry provided digital corner models.) The off-chip inductor value is assumed to have a +/-5%

shift. An S_{11} of -15 dB is set to be the specification. This number is conservative compared to -10 dB because other variations associated with temperature, package, PC board etc. have not been considered. For example, a transceiver chip is supposed to be in a 50 Ω environment. However, the transmission line impedance has variation. Instead of 50 Ω , it is possible to get 46 Ω or 55 Ω due to the variations in PC board manufacturing.

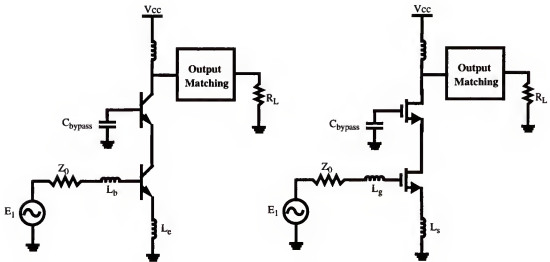


Figure 4-10 Basic BJT and CMOS cascode LNA's used in process variation assessment

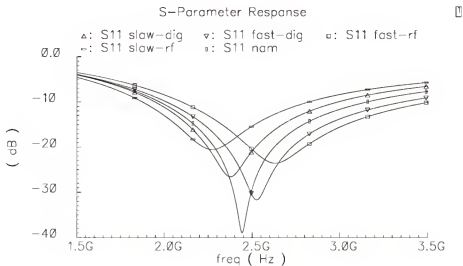


Figure 4-11 S_{11} of MOS LNA, Q of 1, nominal, digital and RF corner models

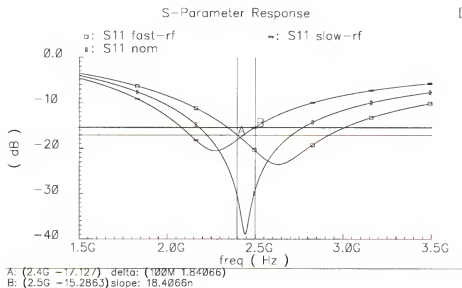


Figure 4-12 Fig. 4-11 redrawn, worst cases (RF-slow and RF-fast) marked, -15 dB spec met

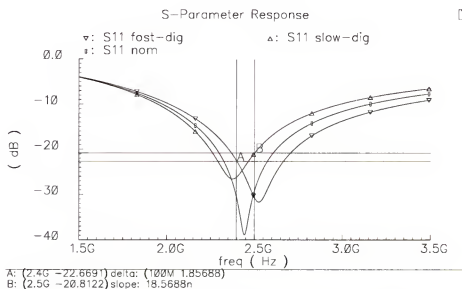


Figure 4-13 Fig. 4-11 redrawn, only the digital corner model results are shown, -15 dB spec met with more than 5 dB of margin

Figures 4-11 and 4-12 demonstrate that for MOS LNA, a Q of 1 is low enough to ensure circuit input matching under process variations. Notice that if the corner models provided by foundry, i.e., the digital corner models are used, the specification is easily met

with more than 5 dB margin, as shown in Figure 4-13. This again demonstrates the importance of proper modeling of corner scenarios. If pure digital corners are used, designer will be tempted to size down the MOS LNA for higher Q, then the input matching requirement may not be met over the real process corners.

Figure 4-14 shows the case with SiGe BJT LNA. The input matching of -15 dB is not accomplished under process variations, even though the nominal Q of BJT LNA is the same as MOS LNA. The reason for this is because, for both real and imaginary part of LNA input impedance, BJT LNA exhibits larger variations.

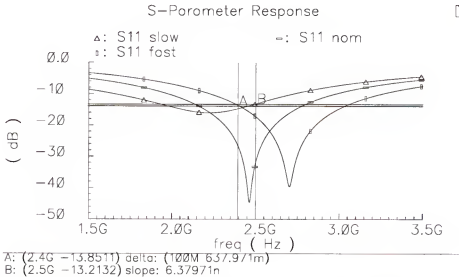


Figure 4-14 S_{11} of BJT LNA, Q of 1, nominal, slow, fast models, 5% off-chip L_b change

For LNA input matching, the real part of the input impedance has to be close to 50 Ω while the imaginary part has to be close to 0. Both LNA's are designed to meet this requirement for nominal cases. Under process variations, the input capacitance change will determine the imaginary part variations. From discussion in previous section, MOS-FET exhibits less capacitance variation than BJT, 14% vs. 21%. On the other hand, for real

part of the input impedance, f_T change is the main factor for variations. MOSFET and BJT have similar worst case f_T variations with BJT slightly worse, 22% vs. 27%. However, for BJT LNA, $g_m f_T / L_c$ only gives part of the real impedance, the other part is base resistance r_b , and the equivalent resistance from r_π (which is in parallel with C_π). From table 4-3, the total base resistance does not change much because the intrinsic base resistance and extrinsic base resistance are moving at opposite direction under process variations. However, r_π does change a lot as β shows more than 150% variations. Therefore, for BJT LNA, both its real and imaginary parts of input impedance have larger variations than their MOSFET LNA counterparts. Consequently the input matching of BJT LNA performs worse under process variations.

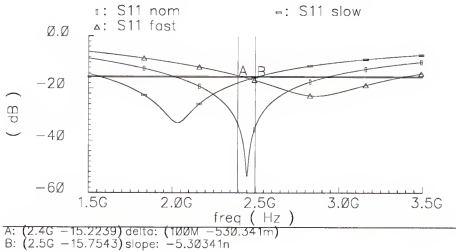


Figure 4-15 BJT LNA with lower input Q, met -15 dB specification

In order for BJT LNA to meet the -15 dB input matching specification, its input transistor has to be resized to lower Q to accommodate the process variations. Figure 4-15 demonstrates that for an input Q of 0.65 or an input capacitance of 1 pF, BJT LNA can meet the input matching specifications. Of course, there is some gain penalty with lower

Q. As shown in Fig. 4-16, BJT LNA transducer gain is 24 dB for a Q of 1 vs. 21.5 dB for a Q of 0.65. In order to accommodate more process variations associated with BJT devices, BJT LNA has to be designed with less Q, consequently less $g_m Q$ product or less gain. This will bring the gain of BJT and MOS LNA's in parity.

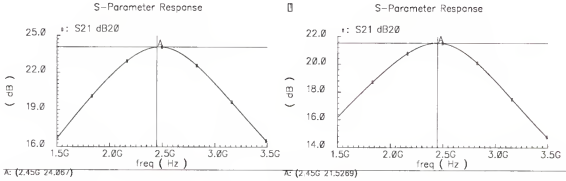


Figure 4-16 Transducer gain of BJT LNA with different input Q's, nominal models: left, Q of 1, right, Q of 0.65.

4.4.2 Impact of Temperature on BJT and CMOS Process Variations

The discussion in last section indicates that CMOS devices exhibits less variations than BJT's. Temperature changes will contribute more to process variations. The characteristics of BJT is closely related to temperature. For example, g_m of BJT circuits is proportional to $1/T$ under ITAT biasing. The characteristics of MOSFET, on the other hand, do not change much compared to BJT devices. To illustrate this, the BJT and MOS LNA's discussed in last section are re-simulated with both temperature and process variations. For simplicity, the 5% off-chip inductor value changes are not considered.

Fig. 4-17 shows the BJT LNA input matching under both temperature (-40 C to 100 C) and process variations for an input Q of 1. The worst cases (slow/fast, 100 C) are

redrawn in Fig. 4-18. Apparently temperature variations make the BJT LNA input matching worse.

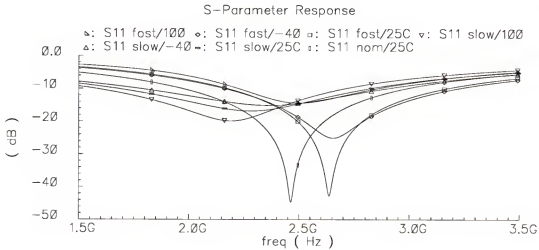


Figure 4-17 BJT LNA (Q of 1) input matching under both temperature and process variations

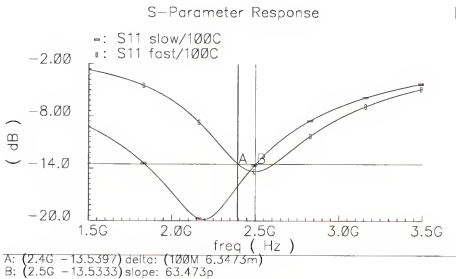


Figure 4-18 Previous figure redrawn, worst cases marked

LNA's with different input Q values are also simulated. Their input matchings are tabulated in tables 4-6 and 4-7. The temperature makes the matching more difficult and the general trend is that when the input Q is lowered, the matching becomes better. However,

for BJT LNA's, there is an optimal Q value. Once this optimal value is reached, further lowering Q will not buy much matching benefit. The reason for this is, for medium Q BJT LNA's, the effect of r_{π} is still in play: the equivalent resistance from r_{π} and $g_m f_T / L_e$ are moving in opposite directions (table 4-3) under process variations and their variations cancel each other out for the real part of the input impedance. Therefore the input matching variation is alleviated. However, at lower Q, the equivalent resistance from r_{π} is essentially 0 because the parallel capacitance is very large. The variations due to r_{π} and $g_m f_T / L_e$ are not cancelled and the S_{11} variations become larger.

Table 4-6 BJT LNA's under both temperature and process variations

Nominal input Q	1.2	1	0.65	0.5
Nominal C_{in}	0.58 pF	0.67 pF	1 pF	1.3 pF
Worst case S_{11} with process variations	-11 dB (slow)	-14.6 dB (slow)	-16.1 dB (fast)	-14.7 dB (fast)
Worst case S_{11} with both T and process variations	-8.5 dB (fast/100C)	-13.5 dB (fast/100 C)	-14 dB (fast/-40C)	-12 dB (fast/-40C)

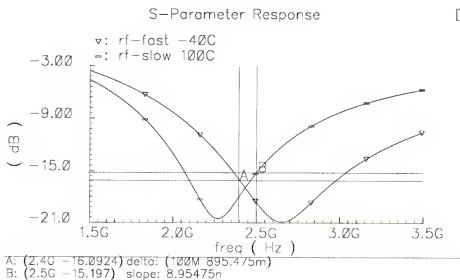


Figure 4-19 S_{11} of MOS LNA with process and temperature variations, only the worst cases are shown, still meet the -15 dB specification

Compared to BJT devices, MOSFET's fare much better under temperature variations as their parameters depend on geometry rather than minority carrier junction. Fig. 4-19 shows the MOS LNA with nominal Q of 1 under both process and temperature variations, plus 5% off-chip inductor variations. Comparing to Fig. 4-12, the input matching is only slightly worse and still meets the -15 dB specification.

Table 4-7 tabulates the input matching of MOS LNA with different nominal input Q under both process and temperature variations (5% off-chip inductor variation is not included). RF corner models are employed in the simulations.

Table 4-7 MOS LNA's under both temperature and process variations

Nominal input Q	4	2	1.5	1	0.5
Nominal C_{in}	0.17 pF	0.34 pF	0.45 pF	0.67 pF	1.3 pF
Worst S_{11} with process variations	-8.3 dB (slow)	-13.72 dB (slow)	-16.8 dB (fast)	-17.3 dB (slow)	-23.5 dB (fast)
Worst S_{11} with both T and process variations	-8.3 dB (slow/25C)	-13.70 dB (slow 100C)	-15.8 dB (fast -40 C)	-17.2 dB (slow 100 C)	-21.2 dB (fast -40C)

As we can see, in order for BJT LNA to exhibit the same input matching as that of MOS LNA under process and temperature variations, its input Q has to be significantly lower. For example, for a requirement of S_{11} less than -13.5 dB, MOS LNA can be designed with a Q of 2 while the largest Q allowed for BJT LNA is only 1, half of that of the MOS LNA. Table 4-8 lists the input matching requirement that mandates the highest Q allowed in both BJT and MOS LNA's.

Table 4-8 MOS and BJT LNA highest Q allowed for different input matching criteria

Input matching requirement	$S_{11} < -8.3$ dB	$S_{11} < -13.5$ dB	$S_{11} < -15$ dB
Highest Q allowed for BJT LNA	1.2	1	Can never meet the criterion
Highest Q allowed for MOS LNA	4	2	1.5

4.5 Conclusion

This chapter compares the BJT RF device of SiGe BiCMOS process and the MOS RF device of CMOS process from a brand new perspective: process/temperature variations. RF chips designed in either process have to withstand these variations to deliver high yield, consequently viable solution in a real world. For RF CMOS to compete as a viable process for WLAN or other RF applications, its process/temperature variations need to be evaluated and compared to those of SiGe BiCMOS processes. The discussion presented in this chapter suggests that, for the CMOS and SiGe BiCMOS processes compared here, CMOS devices exhibit an advantage in terms of process and temperature variations against BJT's. Therefore CMOS RF tuned circuits can be designed with higher Q values than BJT tuned circuits. This will bring the $g_m Q$ products consequently the gain of CMOS and BJT RF circuits close to parity at a given power consumption.

CHAPTER 5

Q-BASED DESIGN APPROACH: AN EXAMPLE

5.1 Q-based Design Approach

5.1.1 Introduction

Most of the RF front-end components in an RF transceiver are tuned circuits. For example, LNA, transmit amplifier (TXA), input and output stages of mixers, and LO buffers. Tuned circuits reject out of band unwanted signals and consume less power than their broadband counterparts. They are desired in all band-limited wireless systems.

Q factor is the most important parameter of tuned circuits, as demonstrated in the analysis of Q of a second order system, and the analysis of input matching of LNA in chapter 4. Based upon this, a Q-based design approach is developed [Okk02]. Low noise amplifiers realized in both BJT and MOS transistors are used to illustrate the Q-based design approach. This approach can easily be extended to the cases of other RF front-end circuits.

5.1.2 The Foundation of Q-based Design Approach

The foundation of Q based design approach is, in order to maintain the overall robustness of a band-limited wireless system, the tuned response of the circuits should be able to withstand component variations (especially in IC circuits). This poses an upper limit on Q. By plotting gain, noise or linearity with respect to Q, the trade-offs among various specifications can be examined and a proper Q can be selected. This will enable us to design the initial transistor sizes and set simulations on the right track.

5.1.3 Starting Point of Q-based Design

The starting point of Q-based design is to identify a unit device. This unit device is then scaled under constant current or other restricting factors depending on design specifications. The Q of the circuit varies with the scaling of the unit device. The important parameters of LNA (Gain, Noise Figure, Linearity) can be plotted versus the Q using MATLAB. A proper selection of Q is made based upon these plots.

It should be emphasized that this analysis is not and should not be viewed as a substitute for computer simulation like SPICE. Rather, it is a great starting point of computer simulation and represents the intelligent part of the design phase. Modern simulation programs provide a powerful tool for analog and RF circuit design. However, jumping into extensive simulation without understanding the behavior of circuit is a dangerous and inefficient practice.

5.2 Cascoded LNA Example

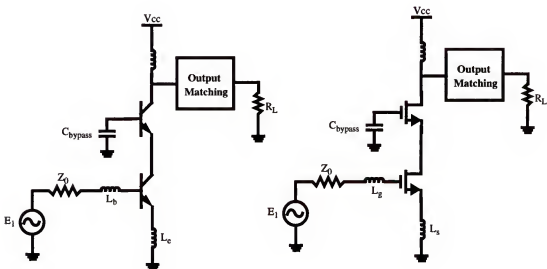


Figure 5-1 BJT (Left) and MOS (Right) cascode LNA's

A single stage cascode amplifier with inductive degeneration is the most popular and successful topology in both CMOS and BJT LNA design. The inductive load is also necessary for dc bias and low loss and noise. Both BJT and MOSFET LNA's are shown again in Fig. 5-1. The Q-based design approach will be applied to them.

The input matching of BJT and MOS LNA's is one of those tuned responses that necessitates the Q-based approach. As analyzed in chapter 4, Q_{in} of the LNA should be sufficiently low to accommodate the process variations. The input impedances of both CMOS and SiGe bipolar LNA's are derived exactly in Appendix B. It can be expressed approximately as

$$Z_{in} = j\omega(L_{in} + L_{deg}) + \frac{1}{j\omega C_{in}} + \frac{g_m}{C_{in}} L_{deg} + r_{in} \quad , \quad (5.1)$$

where L_{in} represents L_b or L_g , and L_{deg} represents the degeneration inductor L_e or L_s , C_{in} represents input capacitance C_π or C_{gs} , r_{in} is the base or gate resistance r_b or r_g , and g_m is the transconductance of the input transistor. An approximation is that, C_μ or C_{gd} is small compared to C_π or C_{gs} , Z_{in} takes the form of a series RLC resonant network, with resonant frequency

$$f_o = \frac{1}{2\pi \cdot \sqrt{(L_{in} + L_{deg})C_{in}}} \quad . \quad (5.2)$$

The quality factor of this network including source resistance Z_0 is

$$Q_{in} = \frac{1}{2\pi f_o C_{in} \cdot (Z_o + 2\pi f_T L_{deg} + r_{in})} \sim \frac{1}{\omega_o C_{in} (2Z_o)} \quad . \quad (5.3)$$

The input matching can not be compromised in a transceiver to boost other specs like noise figure. Some literature claimed that the noise figure of the measured LNA can

be improved if the input matching is, for example, -10 dB instead of -15 dB. This practice will bring risk in a real product scenario where process/component variations tend to shift the input matching. -10 dB S_{11} should be the lower limit for input matching under process, temperature, supply and all other variations rather than an optimal noise matching number.

Having said this, the approximation in equation (5.3) is a very good one. Also, in order for the input to be matched, r_{in} should be much less than 50Ω . This will not be a problem in MOS LNA design as r_g is small and usually can be neglected in the analysis. This however, will be a restriction in BJT Q-based LNA analysis, especially traditional Si BJT where r_b could be large. The number of unit devices should be large enough so that the overall r_b is much less than 50Ω .

5.2.1 Q-based Design for BJT LNA

The unit device is a $10\mu\text{m}/0.5\mu\text{m}$ SiGe npn BJT. A quick dc simulation of the unit device provides the operating point at $I_c = 1 \text{ mA}$. The parameters used for Q based analysis are calculated from the dc operating point analysis.

The frequency used for analysis is 2.45 GHz. A 50Ω system was assumed and the LNA was analyzed at three different dc current levels: 1mA, 4mA and 7mA. I_c is kept constant while Q_{in} (number of stripes) was varied. Base resistance r_b , C_π and C_μ are scaled with respect to Q_{in} . From dc operating point, we have $C_{\mu_unit} = 18.9 \text{ fF}$, $\tau_f = 2.15 \text{ pS}$, $C_{bej} = 148 \text{ fF}$, $r_{b_unit} = 16.6 \Omega$.

How do our bipolar device scale with respect to N, # of stripes? They scale like these:

$$C_\mu = N \cdot C_{\mu, unit} ; \quad (5.4)$$

$$C_{\pi} = g_m \cdot \tau_f + N \cdot C_{bej} ; \quad (5.5)$$

$$r_b = r_{b,unit}/N . \quad (5.6)$$

Since Q_{in} changes with N through C_{π} , these parameters scale with Q_{in} as well. The input is matched to 50Ω using L_b and L_e :

$$\frac{g_m}{C_{\pi}} L_e + r_b = 50 \Omega , \quad (5.7)$$

$$j\omega(L_b + L_e) + \frac{1}{j\omega C_{\pi}} = 0 . \quad (5.8)$$

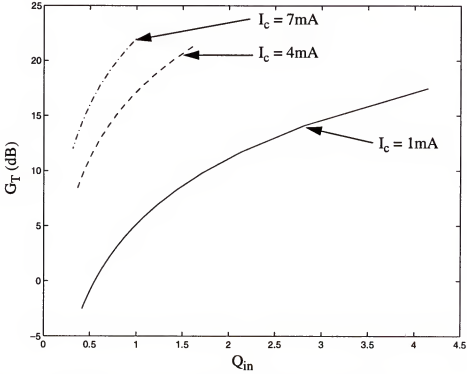


Figure 5-2 Transducer gain vs. Q_{in} for BJT LNA at different bias currents

The transducer gain can be calculated using the following equation. This equation is originally derived [OKK02] for both BJT and CMOS LNA's:

$$G_T = 4g_m^2 R_s Z_o Q_{in}^2 Q_{out}^2 \quad (5.9)$$

Fig. 5-2 shows transducer gain vs. Q_{in} curves using Eq. (5.9). Transducer gain follows a general trend: it increases as Q_{in} increases. Also note that for higher current or higher g_m , Q_{in} can be lower for a given G_T . At 7 mA, Q_{in} is always smaller than 1. This is unique in the case of BJT: C_π depends on current (or g_m), higher current (or g_m) limits the lowest C_π hence highest Q_{in} .

5.2.2 Q-based Design for MOS LNA

The unit device for Q based analysis is a 100 μ m/0.24 μ m nMOS transistor. A quick dc simulation on the unit device provides the operating point at $I_d = 1$ mA. The parameters used for Q based analysis are calculated from the dc operating point analysis.

Once again, the frequency used for analysis is 2.45 GHz, a 50 Ω system was assumed, and the LNA was analyzed at three different dc current levels: 1mA, 4mA and 7mA. The drain current I_d is kept constant while Q_{in} (number of stripes) was varied. C_{gs} and C_{gd} are calculated. The input is matched to 50 Ω through L_g and L_s . Q_{in} of the LNA and the transducer gain are then calculated.

From the dc operating point analysis, we have $C_{gs_unit} = 141.3$ fF, $C_{gd_unit} = 31$ fF, and $\beta_{unit} = 0.0709$. How do MOS devices scale with respect to N, # of stripes? They scale differently compared to BJT devices: the device width W scales with N and

$$C_{gd} = N \cdot C_{gd, unit}; \quad (5.10)$$

$$C_{gs} = N \cdot C_{gs, unit}; \quad (5.11)$$

$$\beta = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \propto N; \quad (5.12)$$

$$g_m = \sqrt{2I_d \cdot \beta} \propto \sqrt{N} . \quad (5.13)$$

Since Q_{in} changes with N through C_{gs} , these parameters also scale with Q_{in} .

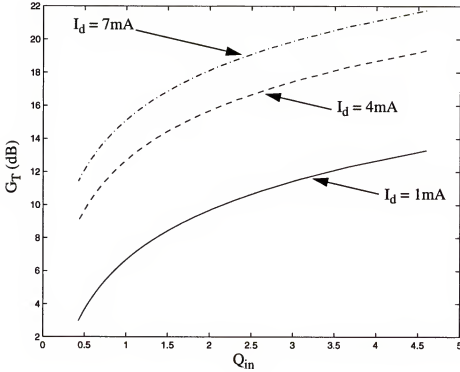


Figure 5-3 Transducer gain vs. Q_{in} for MOS LNA at different bias currents

Note the difference between the MOS and BJT cases is that g_m does not change in BJT LNA while C_{gs} (C_{in}) does not change with current and scales linearly with the number of stripes in a MOSFET. The equation to calculate the transducer gain is still equation (5.9). Fig. 5-3 shows the transducer gain vs. Q_{in} for the MOS LNA at different bias currents. The MOS LNA transducer gain follows the same trend as BJT LNA. G_T increases as Q_{in} increases. However, in the MOS LNA case, Q_{in} depends on the number of stripes only and is not limited by current. At high current levels, MOS LNA power gain can still benefit from higher Q_{in} .

5.3 Q-based Noise Analysis

5.3.1 Introduction to Noise Analysis

Before the Q based noise analysis is discussed, a review of some basic noise analysis concepts is in order. People tend to get lost in the complex algebra of noise analysis, especially RF noise analysis. The underlying mechanism is actually quite simple.

The noise analysis is usually expressed in terms of equivalent input noise [Gra93], which gives the same output noise as the noisy circuit being analyzed, as shown in Fig. 5-4.

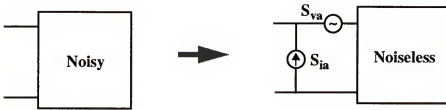


Figure 5-4 Equivalent input noise generators

The noise performance of any two-port network can be represented by two equivalent input noise generators, as illustrated in the figure above. S_{va} , or expressed as $\overline{v_i^2}$, is the noise voltage power spectral density; S_{ia} or expressed as $\overline{i_i^2}$, is the noise current power spectral density. They may be correlated and they represent the noise of the circuit for any source impedance. If the source impedance is $Z_s = R_s + jX_s$, then the noise factor of the circuit can be expressed as

$$F = 1 + \frac{|v_i + i_i \cdot Z_s|^2}{4kTR_s \Delta f} . \quad (5.14)$$

This noise factor can be further expressed, equivalently, in impedance form [Flo01],

$$F = 1 + \frac{R_u}{R_s} + \frac{G_n}{R_s} \left[(R_s + R_c)^2 + (X_s + X_c)^2 \right]; \quad (5.15)$$

or, in admittance form [Gon97]

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s} \left[(G_s + G_c)^2 + (B_s + B_c)^2 \right]. \quad (5.16)$$

Clearly there is minimum F with regard to B_s , when B_s is equal to $-B_c$. In terms of G_s , (if G_u and R_n are non-zero), because the G_u/G_s term decreases but $R_n(G_s+G_c)^2/G_s$ term increases as G_s goes up, there is also a value of G_s for which F is minimized. So, there is an optimal Z_s for which F is minimum, or F_{\min} . The reason for this is quite simple: there are two **competing** factors as impedance Z_s changes, one increases as Z_s increases (G_s decreases), it is proportional to G_u which is related to $\overline{v_{iu}^2} = 4kTG_u\Delta f$; the other decreases as Z_s increases (G_s decreases), it is proportional to R_n which is related to $\overline{v_i^2} = 4kTR_n\Delta f$. Two competing factors in noise contribution result in the existence of a minimum.

Going back to the origins of two noise generators $\overline{v_i^2}$ and $\overline{i_i^2}$, the above discussion is consistent with why they are in the noise analysis in the first place: the noise voltage source represents the case when the source impedance is zero while the noise current source represents the case when the source impedance is infinity. For any other impedances, both noise sources contribute to the equivalent input noise of the circuit. When G_s goes up, noise voltage contributes less while noise current contributes more; when G_s goes down, noise voltage contributes more while noise current contributes less.

The noise analysis can be greatly simplified if one of the noise generators (either voltage or current generator) can be ignored. This is especially true when there is a dominant noise source in the device, as in the case of MOSFET. However, this simplification does not apply to F_{\min} analysis. As pointed out in [Sha97], F_{\min} will approach zero (does not exist) if only one of noise generators is included. It is the existence of both independent voltage noise source and independent current noise source (uncorrelated part) that gives the two competing factors eventually lead to the existence of F_{\min} .

5.3.2 BJT LNA Noise Analysis

First, let's look at the BJT small signal model including noise sources as shown in Fig. 5-5.

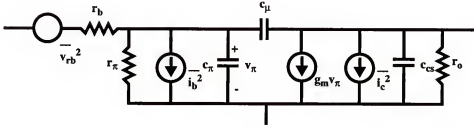


Figure 5-5 BJT small signal model including noise sources

BJT major noise sources include: thermal noise of r_b , $\overline{v_{rb}^2} = 4kTr_b\Delta f$; base shot noise $\overline{i_b^2} = 2qI_b\Delta f$; collector shot noise $\overline{i_c^2} = 2qI_c\Delta f$. Putting this model in the BJT cascode LNA, we can work out the equivalent input referred noise generators $\overline{v_i^2}$ and $\overline{i_i^2}$.

For a BJT LNA, L_b is usually off-chip and effectively without noise. The total input referred noise is

$$v_{ni} = v_i + i_i \cdot (Z_o + j\omega L_b), \quad (5.17)$$

and the noise factor can be expressed as

$$F = 1 + \frac{|\overline{v_{ni}}|^2}{|\overline{v_s}|^2} \quad (5.18)$$

The noise parameters F_{\min} , G_n , $Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}}$ (impedance form) can all be derived once the noise generators $\overline{v_i^2}$ and $\overline{i_i^2}$ are known. They are done in Appendix C. With these parameters at hand, the noise figure and parameters can be plotted with respect to Q_{in} . Figs. 5-6, 7, and 8 are plots of BJT LNA noise figure and minimum noise figure with respect to Q_{in} for different currents.

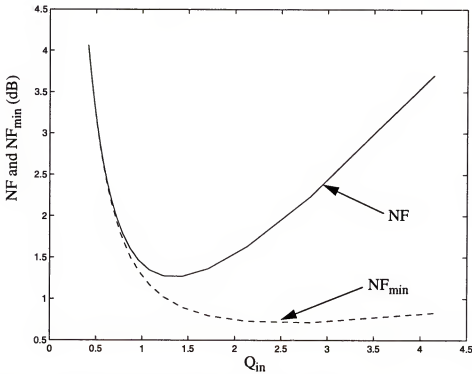


Figure 5-6 BJT Noise Figure, NF_{\min} vs. Q_{in} at $I_c = 1\text{mA}$

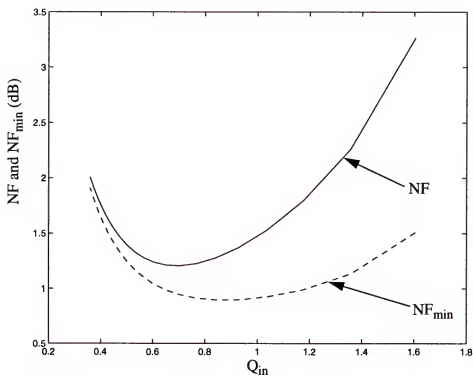


Figure 5-7 BJT Noise Figure, NF_{min} vs. Q_{in} at $I_c = 4\text{mA}$

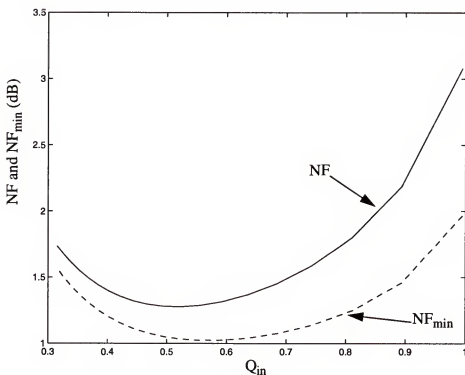


Figure 5-8 BJT Noise Figure, NF_{min} vs. Q_{in} at $I_c = 7\text{mA}$

5.3.3 MOS LNA Noise Analysis

First, let's look at MOS small signal model including noise sources shown in Fig. 5-9. They include thermal noise of gate resistance r_g , $\overline{v_{r_g}^2} = 4kTr_g\Delta f$, gate induced noise $\overline{i_g^2}$ and channel thermal noise $\overline{i_d^2} = 4kT\gamma g_{do}\Delta f$.

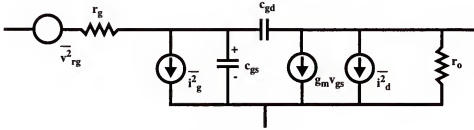


Figure 5-9 MOS small signal model with noise sources

Of these three noise sources, gate resistance is usually very small provided the layout is decent, so the noise of r_g is small. Gate induced noise is also a secondary noise source compared to channel thermal noise which is the dominant noise source in MOS-FET. This is quite different compared to BJT where all three noise sources are equally important.

Using the admittance form, the noise parameters F_{min} , R_n , $Y_{opt} = G_{opt} + jB_{opt}$, can be derived [Sha97]. These are done in Appendix C (the effect of L_s is not considered in the derivation as L_s is usually quite small). With these parameters at hand, using Eq. (5.16), the noise figure can be calculated. In the calculation, the input of the LNA is assumed to be matched with L_g and L_s as shown in Fig. 5-1. Z_s is $50\Omega + j\omega(L_g + L_s)$ and the admittance $Y_s = G_s + jB_s$ is the inverse of input impedance, $1/Z_s$. Figs. 5-10, 11, and 12 show the noise figure with respect to Q_{in} at varying dc bias.

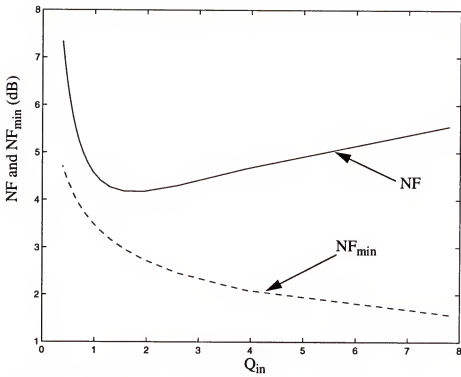


Figure 5-10 MOS LNA NF and NF_{min} vs. Q_{in} , $I_d = 1$ mA (including gate induced noise)

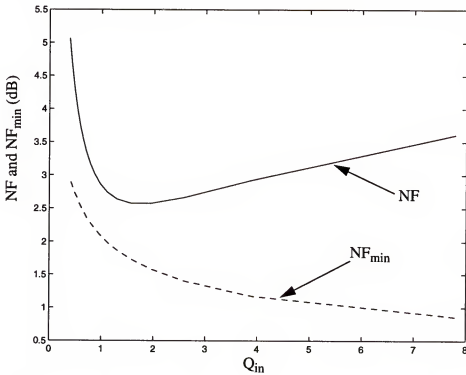


Figure 5-11 MOS LNA NF and NF_{min} vs. Q_{in} , $I_d = 4$ mA (including gate induced noise)

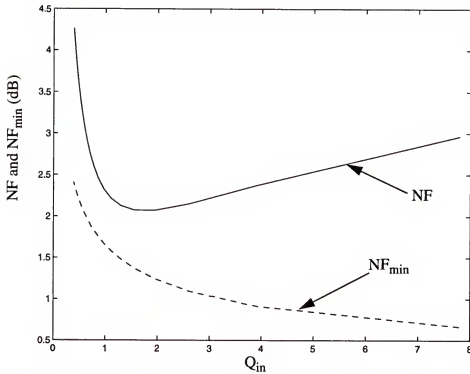


Figure 5-12 MOS LNA NF and NF_{\min} vs. Q_{in} , $I_d = 7\text{mA}$ (including gate induced noise)

5.4 Q-based Linearity Analysis

5.4.1 Introduction to Linearity Analysis

Linearity is as important as noise figure in that linearity sets the upper limit of a radio dynamic range while noise figure sets the lower limit. Amplifiers and mixers deviate from their linear behavior due to violation of the small signal approximation resulting from saturation of the transistor or non-linearity of the diffusion, junction and MOS capacitances. Often IP_3 is used to specify the LNA linearity. Large signal models are necessary for linearity analyses.

For both BJT and MOS cascode LNA's, we assume that the linearity is limited at the input. The output non-linearity like clipping doesn't happen until the input non-linear-

ity is already reached. This is somewhat true if the supply voltage is large enough to leave a sufficient headroom, which is the case in both of our LNA's.

5.4.2 BJT LNA Linearity

For BJT LNA linearity analysis [OKK02], the large signal collector current can be expressed as

$$i_C = I_C + i_c(t), \quad (5.19)$$

where, I_C is the dc component, and $i_c(t)$ is the time varying component.

$$i_C = \beta_o I_B(t) \cong \beta_o I_{BS} e^{\frac{V_{be} + v_{be}(t)}{V_T}} \quad (5.20)$$

$$= \beta_o I_B \left(1 + \frac{v_{be}}{V_T} + \frac{1}{2!} \left(\frac{v_{be}}{V_T} \right)^2 + \frac{1}{3!} \left(\frac{v_{be}}{V_T} \right)^3 + \dots \right) \quad (5.21)$$

$$= (\alpha_o + \alpha_1 v_{be} + \alpha_2 v_{be}^2 + \alpha_3 v_{be}^3 + \dots) \quad (5.22)$$

Assuming that non-linearity is limited by the exponential nature of the collector current, the V_{be} corresponding to the IP_3 is

$$(v_{IP3})_{be} = \sqrt[4]{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} = 2\sqrt{2} V_T = 2.8 V_T. \quad (5.23)$$

This is referred to the base-emitter junction voltage. For IIP_3 , we are interested in referring this voltage to the input of the LNA,

$$(v_{IP3})_{in} = \frac{(v_{IP3})_{be}}{2Q_{in}}. \quad (5.24)$$

The IIP_3 of the BJT LNA is

$$IIP_3 = \frac{(v_{IP3})_{in}^2}{2Z_o} = \frac{V_T^2}{Q_{in}^2 \cdot Z_o} \quad (5.25)$$

The result of Eq.(5.25) is quite simple and somewhat surprising: the IIP_3 is related directly to Q_{in} , not directly to current. Increasing the current may not result in direct increase of linearity. (Of course increasing the current would lower the Q_{in} of LNA.) A more efficient way to boost IIP_3 is to lower the overall Q_{in} . Fig. 5-13 plots the IIP_3 of BJT LNA versus Q_{in} for different current levels: the IIP_3 of higher current LNA can be the same as that of the low current LNA as long as they exhibit the same Q_{in} .

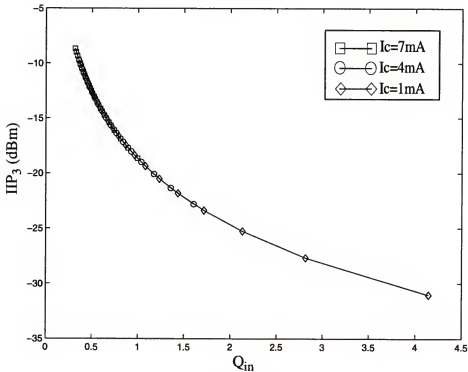


Figure 5-13 BJT LNA IIP_3 vs. Q_{in} , three currents

5.4.3 MOS LNA Linearity

Following the BJT linearity analysis, IIP_3 of the MOS LNA can also be computed. Compared to collect current of BJT which depends exponentially on the input voltage, MOSFET drain current with square law dependency on the input voltage should exhibit better linearity performance. First, let us assume that the transistor drain current fits a perfect square law. The large signal drain current is

$$i_D = I_D + i_d(t), \quad (5.26)$$

where, I_D is the dc component, and $i_d(t)$ is the time varying component: $I_D = \frac{1}{2}\beta V_{GT}^2$ and $V_{GT} = V_{GS} - V_{th}$. The transient large signal drain current can be expressed as

$$i_D = I_D + i_d(t) = \frac{1}{2}\beta[(V_{GS} - V_{th}) + v_{gs}(t)]^2 \quad (5.27)$$

$$= I_D + \beta(V_{GS} - V_{th}) \cdot v_{gs}(t) + \frac{1}{2}\beta[v_{gs}(t)]^2. \quad (5.28)$$

There is no third order term in Eq. (5.28). This says for a perfect square law device, the MOS LNA will not have any third order non-linearity. MOSFET third order non-linearity stems from I_D - V_{gs} deviating from the square law! To the first order, MOSFET's are more linear than BJT's.

Second order effect, like mobility degradation will affect the MOS LNA IP_3 . In [Hua98], a model based on mobility saturation is presented and is implemented to analyze the IP_3 of mixers. The drain current can be expressed as

$$I_D = \frac{1}{2}\beta \frac{[V_{GS} - V_{th}]^2}{1 + \theta(V_{GS} - V_{th})} \quad (5.29)$$

where v_{GS} is the transient $v_{GS}(t)$. The mobility degradation is represented in the denominator term. θ is a technology dependent parameter. For the $0.25\ \mu\text{m}$ CMOS process used in for this dissertation, θ is $\sim 0.7\ \text{V}^{-1}$. Using Taylor expansion and the same approach we used in BJT IP_3 analysis, we have

$$(v_{IP3})_{gs} = \sqrt{\frac{8V_{GT}}{3\theta}} . \quad (5.30)$$

Again, this is referred to the gate source voltage. For IIP_3 , this voltage should be referred back to the input of the LNA, and

$$(v_{IP3})_{in} = \frac{(v_{IP3})_{gs}}{2Q_{in}} . \quad (5.31)$$

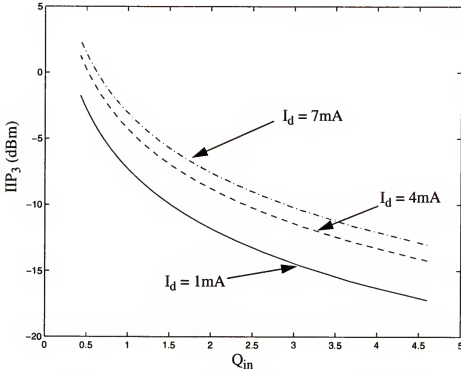


Figure 5-14 MOS LNA IIP_3 vs. Q_{in} , when mobility degradation model is included

The IIP_3 of the MOS LNA is

$$IIP_3 = \frac{(v_{IP3})_{in}^2}{2Z_o} . \quad (5.32)$$

The IIP_3 vs. Q_{in} curves for the MOS LNA are shown in Fig. 5-14. MOS LNA follows the same Q_{in} trend as BJT LNA, i.e., lower Q_{in} leads to better IIP_3 . However, IIP_3 of MOS LNA increases as we increase the current and the MOS LNA generally has better IIP_3 than its BJT counterpart.

5.5 Comparison of CMOS and BJT LNA from Q-based Design Analysis

Q_{in} based design approach is a useful tool to compare different IC technologies for RF circuits and is helpful in gaining insight on the evaluation of technologies for WLAN chip-set or other RF systems.

The analyses in chapter 4 point out that BJT circuits require use of smaller Q than MOSFET circuits to accommodate its larger process and temperature variations. For example, to meet the requirement of input matching of less than -13.5 dB at the same bias current, MOS LNA can have Q_{in} of 2 while BJT LNA can only have Q_{in} of 1. Q_{in} based design approach in this chapter demonstrates that at higher Q , the gain deficiency of MOS circuit is compensated. Also at higher Q , other specifications like noise and linearity for MOS LNA are close to or exceed those of BJT circuits at lower Q . From the rough Q_{in} based design approach estimate in this chapter, at Q_{in} of 2 MOS LNA exhibits gain of 18 dB, IIP_3 of -8 dBm and noise figure of 2.2 dB while at Q_{in} of 0.9 BJT LNA exhibits gain of 21 dB, IIP_3 of -18 dBm and noise figure of 2.2 dB. The trade-off between Q (or process variations) and specifications like gain, linearity shows performance parity between MOSFET and BJT. These illustrate the promising potential of RF CMOS technology.

CHAPTER 6 CMOS FREQUENCY SYNTHESIZER

6.1 Introduction

Oscillator and Frequency Synthesizer (FS) are key elements in a radio system for providing a controlled frequency source for receive signal down conversion and transmit signal up conversion. A simple transistor oscillator, or a voltage controlled oscillator (VCO) does not have the required frequency stability and low phase noise. Therefore, frequency synthesis is necessary to derive the accurate high frequency from a precise low frequency crystal oscillator. Phase Lock Loops (PLL) are often employed to provide the negative feedback in FS [Poz01]. A VCO itself can be viewed as part of the frequency synthesizer, though quite often FS is integrated with other components like amplifiers and mixers into one transceiver chip, and a VCO is left off-chip to ensure system robustness, as in the case of PRISM II.

Fig. 6-1 shows the frequency synthesizer concept diagram in PRISM II radio. The FS is an Integer-N charge pump PLL. It is a popular architecture for wireless FS in many communication systems due to its simplicity. The VCO, crystal oscillator and loop filter are off chip while the rest of the FS is part of the RF/IF Converter transceiver chip. The LO signal out of the VCO is first buffered (As discussed in chapter 3, the LO signal splits into three paths, one of them goes to Rx mixer, one goes to Tx mixer, and one goes to prescaler) before it goes into the frequency divider which comprises a dual modulus divide by 32/33 prescaler and programmable digital counters. The divided signal and the reference

signal are compared by a Phase/Frequency Detector (PFD) which generates the up and down pulse signals to control the charge pump. (A three wire programmable interface sets up all the digital control words for counters, PFD and charge pump.) The output of the charge pump is filtered through an off-chip low pass filter before it enters the VCO as its control voltage. The entire loop forms a negative feedback loop hence stabilizes the VCO output.

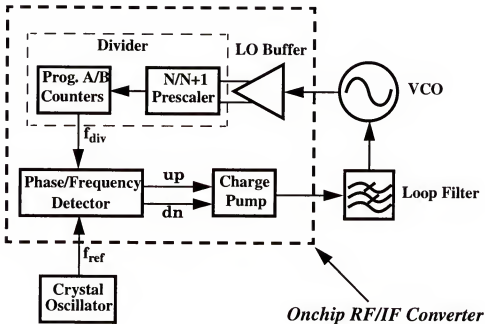


Figure 6-1 Frequency Synthesizer concept diagram

In SiGe FS, the prescaler is made of bipolar transistors while the rest are built using MOSFETs. The CMOS FS design focused on divide by 32/33 prescaler and simplified the other low frequency digital part of the FS.

6.2 CMOS Frequency Synthesizer Overview

Fig. 6-2 shows the CMOS synthesizer top cell. Due to limited resources, the three wire interface is not included. The division ratios (bits) of A counter and B counter of the

programmable counters are fixed except the first bit of each counter. Consequently this CMOS FS can only change division ratio by 2 bits. (through 2 pins: A, the first bit of A counter and B, the first bit of B counter.)

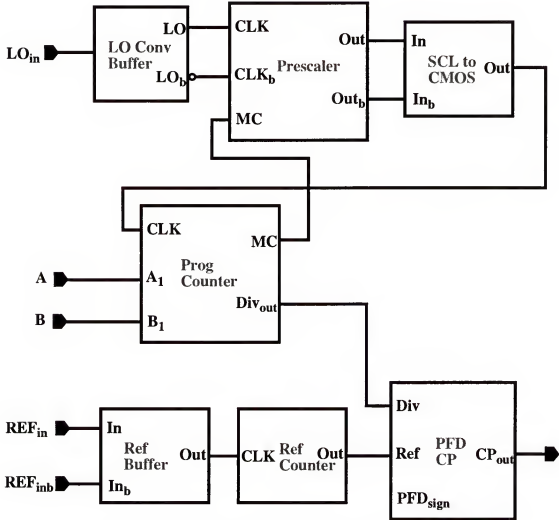


Figure 6-2 CMOS Frequency Synthesizer top schematic

The reference signal comes from an off-chip 44 MHz crystal oscillator, the final reference frequency at PFD was set to be 250 kHz. A reference buffer and counter are designed to divide 44 MHz reference signal down to 250 kHz. To reduce cross coupling, V_{cc} lines for different blocks use separate pins.

6.3 CMOS Prescaler Design

6.3.1 Prescaler Top Schematic

Fig. 6-3 shows the prescaler top schematic.

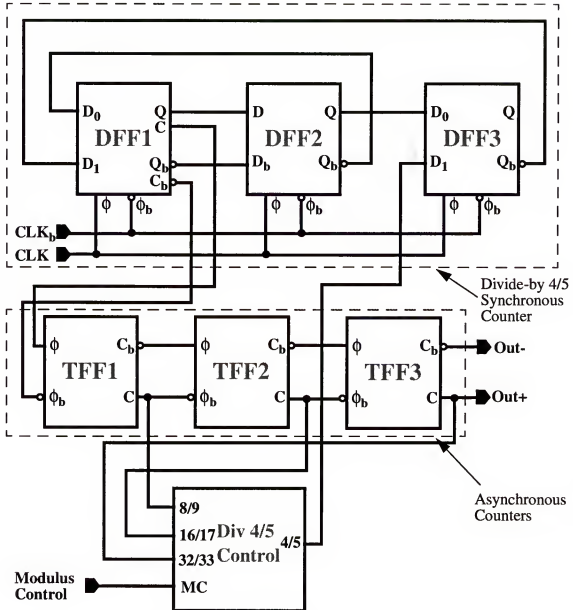


Figure 6-3 Divide-by-32/33 prescaler top schematic

The prescaler is a dual module divide by 32/33 analog divider. It consists of a divide by 4/5 synchronous counter followed by three asynchronous counters. These analog counters are designed using Source Coupled Logic (SCL) [Hun00, Flo01].

6.3.2 Divide by 4/5 Synchronous Counter

The concept of divide by 4/5 is illustrated in Fig. 6-4, which is similar to divide by 2/3 mechanism [Yan98, Yan99]. When MC is high, this circuit divides by 4; when MC is low, it divides by 5.

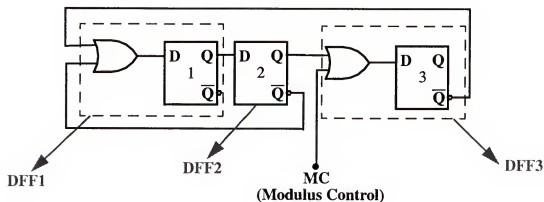


Figure 6-4 Divide by $\frac{4}{5}$ concept

In the analog implementation of divide by 4/5 synchronous counter, the OR function and the D-flip flop (DFF) are combined into one circuit block, called OR_DFF. In Fig. 6-3, DFF1 and DFF3 are OR_DFF's while DFF2 is a simple DFF.

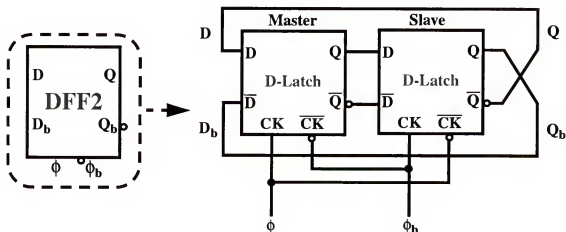


Figure 6-5 D Flip Flop of synchronous counter schematic

Fig. 6-5 shows the schematic of DFF2, or a D-flip flop, which is a master slave configuration of two SCL D latches. Fig. 6-6 shows the schematic of SCL D latch. PMOS loads instead of resistive loads are used for SCL [Hun00].

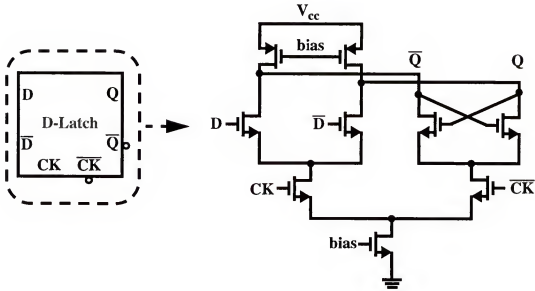


Figure 6-6 SCL D Latch schematic

The OR DFF schematic is shown in Fig. 6-7. Unlike the simple DFF case where the input signals are differential and symmetrical, the OR function requires that the input signals compare their levels with a reference voltage to determine whether the signal is high or low. In SCL logic, the signal swing is low and its DC value tends to shift around due to process variations or changes in V_{CC} , load resistance or DC bias voltage. On the other hand, it is not an easy task to get an accurate reference voltage on-chip. A solution to this is the circuitry that sets up the reference voltage V_B shown in Fig. 6-7, which has been also used in the SiGe transceiver chip.

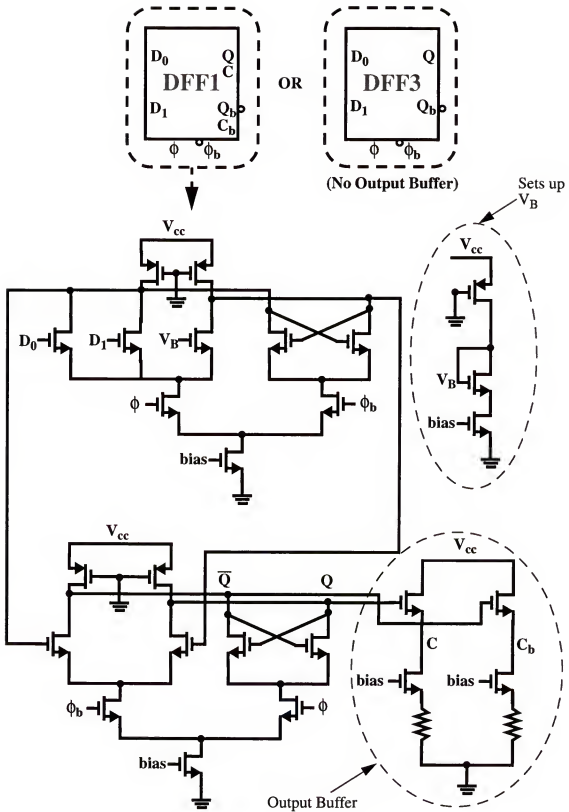


Figure 6-7 OR DFF schematic

The circuit that sets up the reference voltage V_B on-chip works this way. The current source M_{21} has half the width of the latch current source M_9 . Therefore, it has half of the current of the latch while maintain the same load and V_{CC} . The logic high of the latch is V_{CC} , the logic low is $V_{CC} - I R_{load}$, and V_B is $V_{CC} - I R_{load} / 2$, right in the middle of logic high and low, independent of supply voltage, current, or load resistance variations. The output buffer in Fig. 6-7 is only present in DFF1 (not in DFF3), which interfaces with the asynchronous counters. The buffer helps to isolate the synchronous counter from the asynchronous counters and to set up the DC bias of the first divider of the asynchronous counters.

6.3.3 Asynchronous Counter

The asynchronous counter consists of three cascaded 2:1 dividers with dual phase inputs and outputs. Each divider, shown in Fig. 6-8, comprises two SCL latches in a master slave configuration. TFF represents TFF1, or TFF2, or TFF3. Cascading two level sensitive latches in a master slave configuration results in an edge triggered DFF. Connecting the outputs of a DFF back to its inputs with inverted phase forms a 2:1 divider [Flo01].

An output buffer is used in every TFF divider to interface with the following stage and the Modulus Control (MC) logic circuit. The latch assumes the same schematic as in the DFF of the synchronous counter, however, the transistor sizes are different. Each transistor in every divider is optimized for low current consumption and a high operating frequency range.

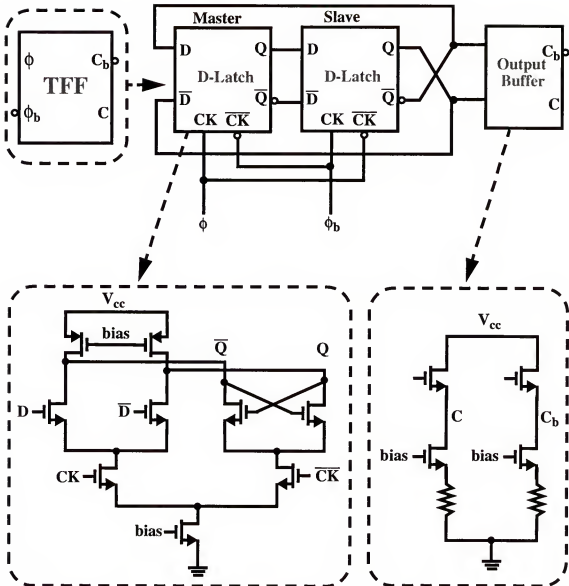


Figure 6-8 Asynchronous counter schematic

6.3.4 Divide-by-4/5 Control

A dual modulus (large numbers like 32/33, 128/129) prescaler usually consists of a dual modulus (small numbers like 2/3, 4/5) synchronous counter followed by an asynchronous counter. The synchronous counter and asynchronous counter need to work together to achieve the dual modulus operation.

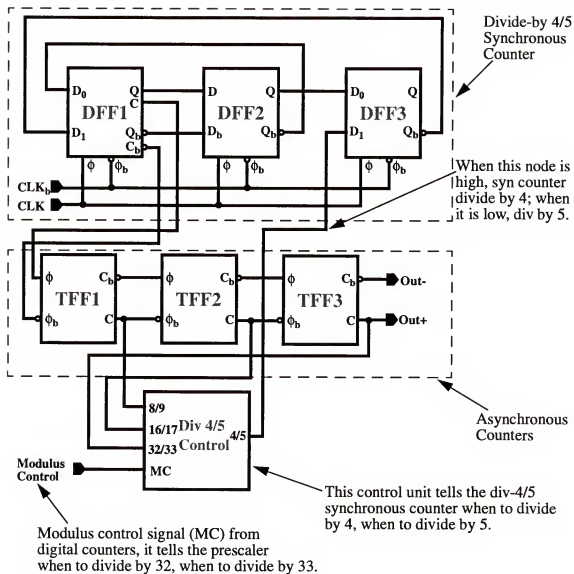


Figure 6-9 Divide-by-32/33 prescaler top schematic redrawn

Even number divisions are easy to realize and understand. When the synchronous counter divides by 4, the prescaler naturally divides by 32. For the odd number division, Divide-by-4/5 Control unit has to come into play. For example, in the prescaler, redrawn in Fig. 6-9, the divide by 33 action is accomplished by seven cycles of divide by 4 and one

cycle of divide by 5. Divide-by-4/5 Control is the circuit block that tells the synchronous counter when to divide by 4, and when to divide by 5.

The Modulus Control (MC) signal from digital counters (A/B counters) is one of the inputs of Divide-by-4/5 Control (MC node in Fig. 6-9). It tells the prescaler which division ratio it is supposed to pick, 32 or 33. The 4/5 node is the output of Divide-by-4/5 Control, as well as the input to the synchronous counter. When 4/5 is high, the synchronous counter divides by 4; when 4/5 is low, the synchronous counter divides by 5.

6.4 Rest of the Frequency Divider

As mentioned earlier in Fig. 6-1, a dual modulus prescaler is one part of the divider of a frequency synthesizer (FS). In the SiGe FS, the rest of the divider is designed using MOSFETs, and those circuits are simplified and ported into the CMOS FS.

6.4.1 SCL to CMOS Converter

The divided down signals out of the prescaler are still analog SCL signals. An SCL to CMOS converter in Fig. 6-10 converts them into CMOS digital signals. To use the 3V supply voltage in the system, high voltage MOSFETs (3.3V devices) are employed.

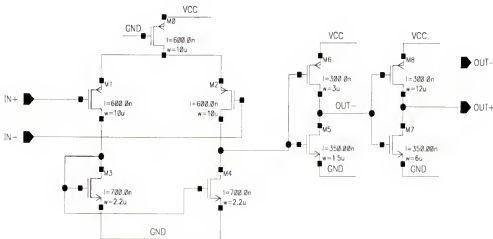


Figure 6-10 SCL to CMOS converter schematic

6.4.2 Digital Counters (A/B Counters)

The total division ratio for a dual module prescaler with A/B counters is $NB+A$, where the prescaler divides by $N/N+1$, and A and B are counts of A, B counters. A and B counters are sometimes called program counter and swallow counter, respectively.

Fig. 6-11 illustrates the concept of a divider with a dual modulus prescaler and A and B counters. The output of the prescaler clocks both A and B counters. The prescaler is set to divide by $N+1$ first and the divider chain divides by $A(N+1)$. When the swallow (A) counter is full, it ceases counting and sets the prescaler to divide by N through Modulus Control (MC) signal. Now only the program (B) counter is clocked but by this time the program (B) counter has already counted up to A. (For A, B counters to work properly, B must always be larger than A.) So the divider chain divides by $(B-A)N$ until the program (B) counter is full. When program (B) counter is full, it resets both the swallow and programmable counters and the cycle repeats. The overall division ratio of the divider chain is, therefore, $(B-A)N + A(N+1) = NB + A$.

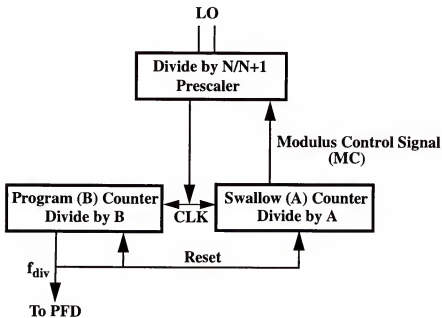


Figure 6-11 Divider with dual modulus prescaler concept diagram

In PRISM II radio, RF is from 2.4 GHz to 2.48 GHz, IF is 374.25 MHz, which results in an LO of 2025 MHz to 2105 MHz. The final synthesizer reference frequency is set to 250 kHz out of system considerations. The total division ratio is from 8100 to 8420. The off-chip crystal oscillator comes in at 44 MHz. A reference counter divides it down to 250 kHz. The total division ratio is fixed at 176 ($44 \text{ MHz} / 250 \text{ kHz} = 176$) for the reference counter.

The serial interface was not included in this design. The total division ratio is set for an LO around 2082 MHz. This number is picked to be in the middle of the VCO frequency range. The prescaler is divide-by 32/33, B is set to be 260 (or 261), while A is set to be 8 (or 9). The total division ratio is $NB+A=8328, 8329, 8360, 8361$, the corresponding LO frequencies are, 2082 MHz, 2082.25 MHz, 2090 MHz, 2090.25 MHz. This helps to test the synthesizer functionality in the absence of serial interface.

6.4.3 Phase Frequency Detector (PFD) and Charge Pump (CP)

The final Charge Pump (CP) current for PRISM II is 1 mA and the loop bandwidth of the low pass filter is 1 kHz. The whole PLL simulation is very time consuming at SPICE level. The PFD and CP are simulated separately with respect to other circuits of the PLL.

The PRISM II off-chip loop filter components were used in the simulation as shown in Fig. 6-12. Two input signals are square waves with a period of $4 \mu\text{s}$ (250 kHz). They both have rise and fall time of 1 nS, and the pulse width is 15 nS. There is a phase difference between the two pulses. Transient voltages on CP output node and VCO V_{CTRL} node are monitored as outputs.

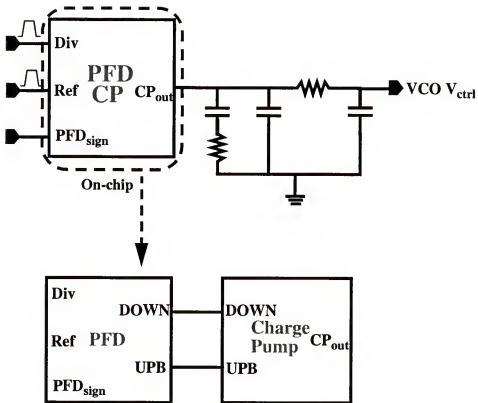


Figure 6-12 PFD and CP Simulation top schematic

6.4.4 PFD and CP Design

Simple CP and PFD are implemented here and shown in Figs. 6-13 and 6-14. The PFD consists of 4 NAND RS flip-flops. The basic operation is: the reference pulse causes the output to change in a positive direction unless the output is already positive; the divider pulse causes a negative transition unless the output is already negative. “sign_pfd” is a multiplexer (MUX) circuit controlled by the word “PFD_sign”. The MUX can reverse the outputs of the PFD, i.e., UP to DOWN, DOWN to UP, which keeps the whole phase-locked loop a negative feedback loop even if the VCO sign is reversed. (VCO gain may have a negative sign, i.e., the output frequency goes down as the control voltage goes up.) The delay circuitry is used to correct the deadzone problem of the PFD [Hun00].

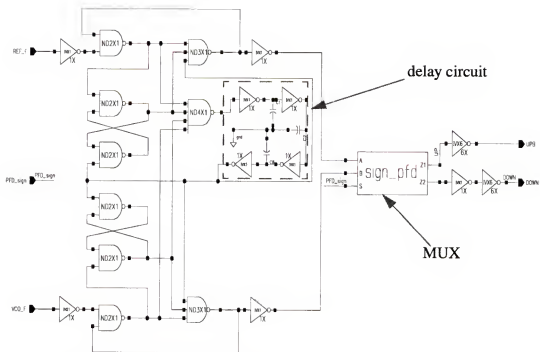


Figure 6-13 Phase Frequency Detector (PFD) schematic

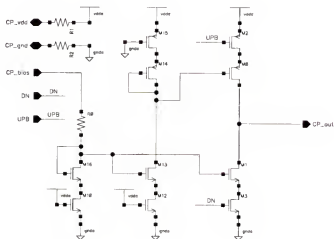


Figure 6-14 Charge Pump (CP) schematic

6.5 CMOS Frequency Synthesizer Measurement Results

As mentioned, a frequency Synthesizer (FS) is the most complex circuit in the RF transceiver chip. The CMOS FS has thousands of transistors even though its digital parts

have been greatly simplified. From a research point of view, it is prudent to build a stand-alone silicon before embark on the task of building the full chip. A CMOS FS is built in a $0.25\text{ }\mu\text{m}$ CMOS and its silicon measurement results are shown here. Fig. 6-15 shows a micro-photograph of the CMOS synthesizer. The die size is $1300\text{ }\mu\text{m}$ by $1800\text{ }\mu\text{m}$.

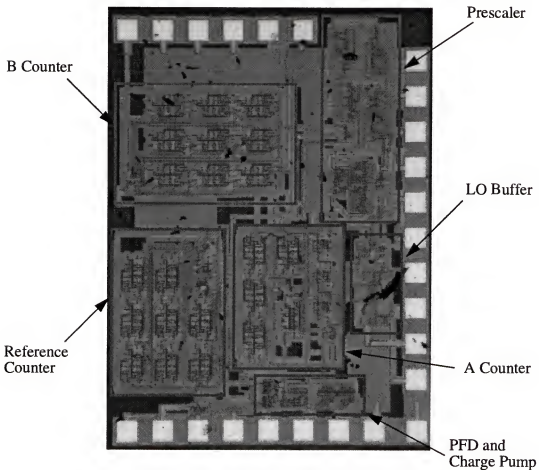


Figure 6-15 A Micro-photograph of CMOS Frequency Synthesizer

6.5.1 CMOS Synthesizer Output Spectrum

Figs. 6-16 to 6-19 depict the output spectra of the CMOS synthesizer. With the change of a 2 bit word: the first bit of A counter ($A = 8$ or 9), and the first bit of B counter

(B = 260 or 261). The output frequency is (NB+A) times the reference frequency 250 kHz.

For example, with A = 8, B = 261, $f_{\text{out}} = (261 \times 32 + 8) \times 250 \text{ kHz} = 2.09 \text{ GHz}$.

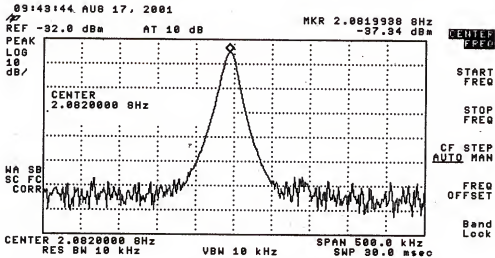


Figure 6-16 CMOS Synthesizer output locked at 2.082 GHz (A=8, B=260)

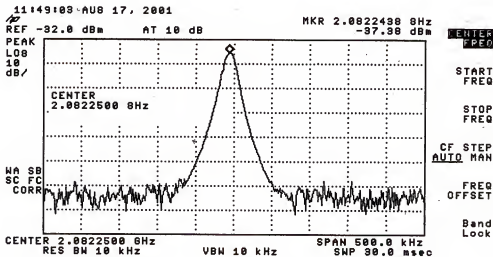


Figure 6-17 CMOS Synthesizer output locked at 2.082250 GHz (A=9, B=260)

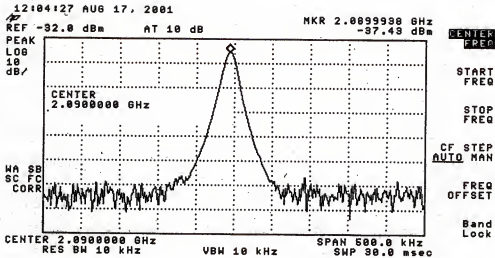


Figure 6-18 CMOS Synthesizer output locked at 2.090 GHz (A=8, B=261)

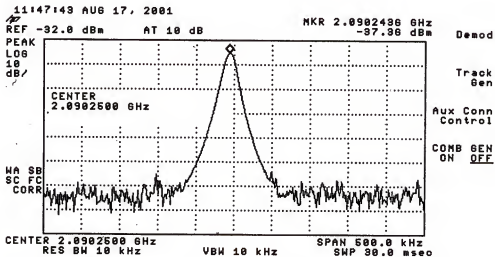


Figure 6-19 CMOS Synthesizer output locked at 2.090250 GHz (A=9, B=261)

6.5.2 Summary of FS Performance

Table 6-1 summarizes the CMOS and SiGe synthesizer performance. In PRISM II, the loop bandwidth is 1 kHz. Phase noise from the VCO contributes most to the overall

synthesizer phase noise above 1kHz. The rest of the phase noise comes from the divider, charge pump, and loop filter. The close-in phase noise of the CMOS and SiGe synthesizers is close: it is at -80 dBc/Hz and -82.7 dBc/Hz at 10 kHz offset, respectively. The CMOS prescaler consumes more current than its SiGe counterpart because it needs more current than BJT prescaler to function at high frequencies.

Table 6-1 CMOS and SiGe RF Synthesizer Comparison Table

Parameters	CMOS	SiGe
LO Frequency	2082 MHz	1800 to 2220 MHz
Reference Frequency	44/0.25 MHz	same
A counter division	8 or 9	0-127
B counter division	260 or 261	3-2047
Charge Pump Current	1 mA	same
Prescaler Current	9.7 mA	6 mA
Phase Noise (10kHz)	-80 dBc/Hz	-82.7 dBc/Hz

CHAPTER 7 CMOS TRANSMITTER BUILDING BLOCKS AND TRANSCEIVER DESIGN

7.1 CMOS Transmitter Chain

The transmitter consists of an up-conversion mixer (Tx mixer) and a transmitter amplifier (TXA), or a pre-PA amplifier. Usually noise figure is not a concern in transmitter design while linearity and gain are important. Recalling the system overview in chapter 3, the output of Tx mixer goes off-chip, then back on-chip to TXA input. A BPF may be placed after Tx Mixer, prior to TXA, to attenuate various spurious components like LO, image, and their harmonics out of the Tx mixer output. Alternatively, if the TXA output goes to another BPF before PA, this BPF can be omitted, which is the case in PRISM II, as illustrated in Fig. 7-1.

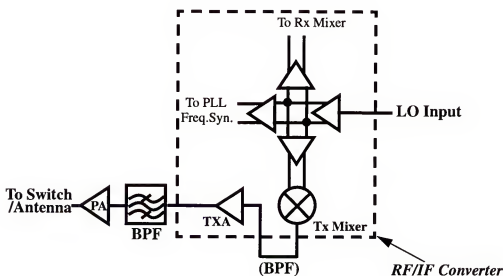


Figure 7-1 PRISM II Transmitter Chain concept diagram

7.2 CMOS Tx Mixer Design

The CMOS Tx mixer uses the same double balanced Gilbert cell topology as the Rx mixer. The design is challenging in terms of meeting both the gain and linearity specifications. The output of Gilbert cell mixer can be viewed as two current sources 180° out of phase to each other at RF frequency (Fig. 7-2). It is inherently differential, while in our system Tx mixer output has to go off-chip single-endedly with $50\ \Omega$ termination. Combining the two opposite phase current together and delivering it into the load becomes a key issue in designing the Tx mixer.

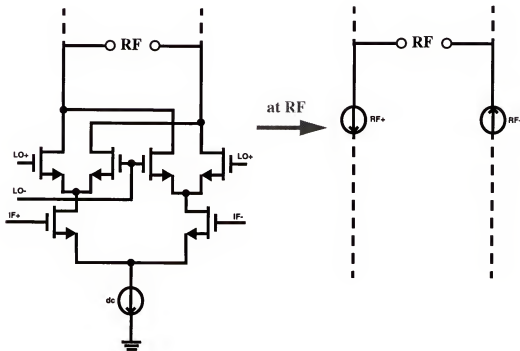


Figure 7-2 Differential output of Gilbert Cell mixer

At low frequencies, a current mirror load utilizing p-type devices can be implemented as a current combiner. This, however, does not work at RF where the impedance has a large imaginary part due to parasitics. (If the two current sources are not combined

and only one of the differential outputs is used, then there is an immediate 3 dB loss in gain.) Most of the RF differential to single-end converters [Won94, Raz99] employ LC resonant networks, as shown in Fig. 7-3.

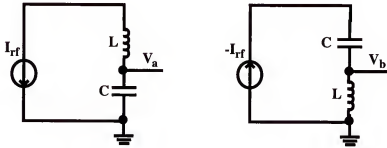


Figure 7-3 LC resonant tank for differential to single-end conversion

If the LC networks resonate at the RF frequency and the Q of the LC networks are the same, then V_a and V_b will be in phase: $V_a \sim (I) (1/sC)$, $V_b \sim (-I) (sL)$, so, $V_a/V_b \sim (-1) / (s^2 LC) \sim 1$ at resonance and $V_a - V_b = 2I(1/sC) = 2I(sL)$. However, it is very hard to build a decent differential to single end converter at RF frequencies. And often, it requires more area and circuit complexity while the advantage in gain is only around 1.5 dB in reality (3dB in theory). This has led to the Tx mixer core shown in Fig. 7-4, where output is derived from only one leg. Unlike a conventional Gilbert cell where a current source at the bottom provides the bias for the whole circuit, this Tx Mixer is biased through its input IF transistors. (The current source will affect the linearity by limiting the leg room of the mixer.)

Table 7-1 summarizes the simulation results of the above mixer. It demonstrates good linearity which prompted the selection of the mixer as the final Tx mixer in CMOS transceiver. The missed gain target in this Tx mixer is planned to be compensated in the TXA design so that the overall transmitter gain will still meet the specifications.

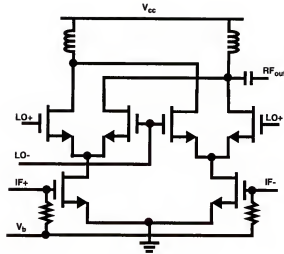


Figure 7-4 CMOS Tx mixer core schematic

Table 7-1 Summary of CMOS Tx Mixer Simulation Results

	CMOS (Simulated)	SiGe (Measured)	PRISM II Specs
LO/IF Frequency	2.1 GHz/375 MHz	same	same
Power Gain	5 dB	9 dB	9 dB
Core Icc	16 mA	10 mA	11 mA
Output matching (RF)	< -10 dB	-27.4 dB	VSWR < 2:1
OP _{1dB}	-5.5 dBm	-3.5 dBm	-6 dBm
OIP ₃	+3 dBm	Not Avail.	+4 dBm
LO to RF feedthru	-33 dB	-35 dB	Not Avail.
IF to RF feedthru	-41 dB	Not Avail.	Not Avail.

7.3 CMOS Transmitter Amplifier

The Transmitter Amplifier (TXA) is a single stage, common source cascode configuration, very similar to LNA topology. Primary design goals include output power greater than +6dBm, gain above 15 dB while limit current consumption as much as possible.

7.3.1 CMOS Transmitter Amplifier Schematic

Fig. 7-5 shows the schematic of the CMOS transmitter amplifier. The output uses the same π matching network as the LNA. Power gain is the primary design goal of the

TXA and as mentioned earlier, noise figure is not a big concern. Therefore, the inductive degeneration was not present (There is no stability problem or linearity degradation associated with this, at least in simulation.) and an on-chip 3.2 nH inductor was included for input matching.

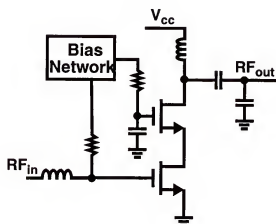


Figure 7-5 TXA schematic

7.3.2 TXA Simulation Results

Table 7-2 summarizes the TXA simulation results and compares them with the SiGe specifications. The gain is around 20 dB while the total current is below 16 mA. The gain deficiency at Tx mixer stage is compensated here.

Table 7-2 Summary of CMOS TXA Simulation Results ($f_0 = 2.45$ GHz)

	CMOS (Simulated)	SiGe (Measured)	PRISM II Specs
Power Gain	19.9 dB	16.7 dB	15 dB
OP _{1dB}	+6 dBm	+7 dBm	+6 dBm
OIP ₃	+17 dBm	Not Avail.	+16 dBm
TXA I _{cc}	16 mA	15 mA	11 mA
Input Matching	< -10 dB	< -10 dB	VSWR < 2:1
Output Matching	< -10 dB	< -10 dB	VSWR < 2:1

7.4 CMOS RF Transceiver (TRx) Design

The CMOS TRx was designed to have the similar size and pinout as that of the SiGe bipolar version (Table 7-3) so better comparison can be made for two technologies.

Table 7-3 CMOS and SiGe Transceiver Comparison

Parameters	CMOS	SiGe
Package	44 pin MLF	same
Components	LNA, Rx and Tx Mixers, PA driver, Synthesizer.	same, plus ITAT/PTAT bias, control pins.
Chip Area	2500 μm X 2500 μm	2563 μm X 2563 μm
Pad separation	150 μm	136 μm

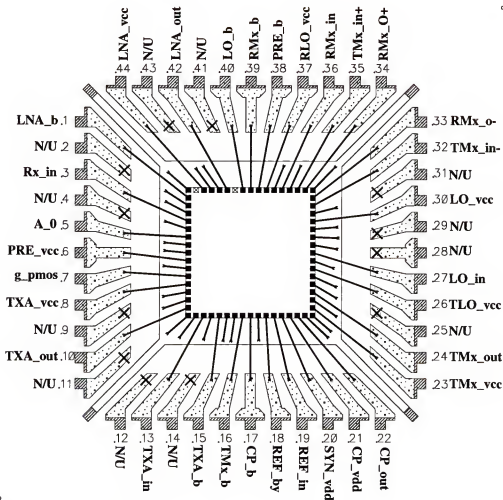


Figure 7-6 CMOS TRx pinout

Fig. 7-6 shows the CMOS TRx pinout and bonding diagram. Table 7-4 details the definition of every pin and compare them to the pinout of SiGe TRx.

Table 7-4 CMOS Transceiver Pinout

Pin #	Name	CMOS Definition	SiGe Definition
1	LNA_b	LNA bias, current source	used for LNA vcc
2	N/U	Not Used	GND
3	Rx_in	LNA input	same
4	N/U	Not Used	Vcc for Bias Circuitry
5	A_0	Synthesizer A counter first bit	LNA H/L gain control
6	PRE_vcc	Prescaler vcc	Power Enable 2
7	g_pmos	Prescaler pMOS load gate voltage	Power Enable 1
8	TXA_vcc	TXA vcc	same
9	N/U	Not Used	GND
10	TXA_out	TXA output	same
11	N/U	Not Used	GND
12	N/U	Not Used	TX_vcc1
13	TXA_in	TXA input	same
14	N/U	Not Used	GND
15	TXA_b	TXA bias, current source	LE, synthesizer load enable
16	TMx_b	Tx Mx bias, current source	DATA, synthesizer data in
17	CP_b	Charge pump current bias	CLK, synthesizer data clock
18	REF_by	Synthesizer reference gnd	same
19	REF_in	Synthesizer reference in	same
20	SYN_vdd	Synthesizer vdd	same
21	CP_vdd	Charge pump vdd	same
22	CP_out	Charge pump output	same
23	TMx_vcc	Tx Mx vcc	same
24	TMx_out	Tx Mx output	same
25	N/U	Not Used	Tx Mx vcc2
26	TLO_vcc	Tx Mx LO driver vcc	same
27	LO_in	LO input	same
28	N/U	Not Used	Single ended LO gnd, diff input

Table 7-4 CMOS Transceiver Pinout

Pin #	Name	CMOS Definition	SiGe Definition
29	N/U	Not Used	LO vcc
30	LO_vcc	LO vcc	Rx LO driver vcc
31	N/U	Not Used	GND
32	TMx_in-	Tx Mx diff input -	same
33	RMx_o-	Rx Mx diff output -	same
34	RMx_o+	Rx Mx diff output +	same
35	TMx_in+	Tx Mx diff input +	same
36	RMx_in	Rx Mx RF signal input	same
37	RLO_vcc	Rx LO driver vcc	Prescaler vcc
38	PRE_b	Prescaler current bias	ITAT bias resistor 1
39	RMx_b	Rx Mx current bias	PTAT bias resistor
40	LO_b	LO buffer bias	Bias circuitry vcc
41	N/U	Not Used	ITAT bias resistor 2
42	LNA_out	LNA output	same
43	N/U	Not Used	GND
44	LNA_vcc	LNA vcc	same

Table 7-5 compares the component area of different circuit blocks of CMOS and SiGe transceiver. This is a very rough estimation from layout since most of the circuit layout is not rectangular and the boundary of different blocks is hard to define. The LO drivers for RMx and TMx are counted as part of the respective mixers. The areas for different blocks are close for CMOS and SiGe transceivers though their layout is quite different.

Table 7-5 CMOS and SiGe transceivers component area breakdown

	CMOS	SiGe
LNA (mm^2)	0.44	0.36
Rx Mixer (mm^2)	1.19	0.97
Tx Mixer (mm^2)	1.03	0.81
TXA (mm^2)	0.36	0.28
Synthesizer (mm^2)	1.1	1.12
LO Buffer (mm^2)	0.28	0.09
Total Area (mm^2)	6.25	6.55

Table 7-6 summarizes the simulated CMOS transceiver performance. An immediate observation is that the current consumption of CMOS TRx is 30% more than SiGe one. Most of this is due to the low g_m/I ratio of CMOS compared to SiGe bipolar. A more advanced technology (0.18 μm vs. 0.25 μm CMOS) is expected to alleviate this problem.

Table 7-6 2.4 GHz CMOS Transceiver Performance

	CMOS (Simulated or Measured)	SiGe (Measured)
LNA (Gain/NF/ IIP ₃ /Current)	15 dB / 3 dB 0 dBm / 8 mA	16 dB / 3 dB -2 dBm / 7 mA
Rx Mixer (Gain/NF/IIP ₃ /Current)	8 dB / 11 dB + 3 dBm / 12 mA	8 dB / 8 dB + 6 dBm / 10 mA
Tx Mixer (Gain/OP _{1dB} /Current)	5 dB / -6 dBm 16 mA	9 dB / -4 dBm 10 mA
TXA (Gain/OP _{1dB} /Current)	19 dB / +6 dBm 16 mA	16 dB / +7 dBm 15 mA
Synthesizer (Phase Noise/ Prescaler Current)	-80 dBc/Hz (10 kHz) 10 mA	-83 dBc/Hz (10 kHz) 6 mA
Total Current: Excl. offchip (Rx/Tx)	Rx: 41 mA Tx: 56 mA	Rx: 32 mA Tx: 41 mA

CHAPTER 8

CHARACTERIZATION OF CMOS TRANSCEIVER AND WLAN RADIO

8.1 Measurement of CMOS RF Transceiver

The main purpose of this dissertation is to explore the feasibility of designing the RF transceiver of PRISM II chipset using a CMOS technology. The realization of the whole transceiver (TRx) in CMOS is a critical milestone of this dissertation. The CMOS TRx was designed in the TSMC 0.25- μm CMOS process. Fig. 8-1 shows a picture of the fabricated silicon.

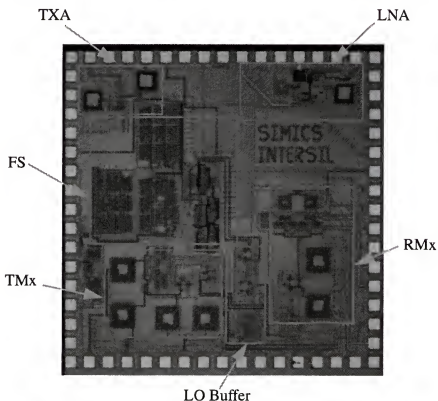


Figure 8-1 Micro-photograph of CMOS RF transceiver chip

The chip was packaged in the 44 pin MLF package as planned and put on the same evaluation board used for SiGe chip. The values of some off-chip components are changed to accommodate the matching of CMOS transceiver. The RF characteristics of chip were measured and compared to simulation and SiGe bipolar chip.

As shown in Fig. 8-2, most of the individual RF circuits in the RF transceiver can be tested separately.

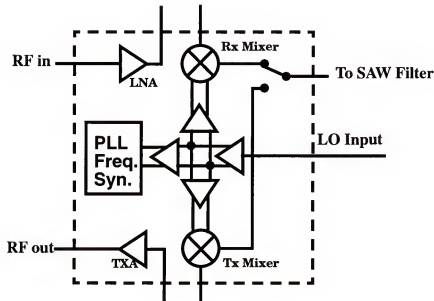


Figure 8-2 RF/IF Converter Chip Components

8.1.1 LNA measurement results

The performance of this LNA is worse than the previous stand-alone one. A change was made in this LNA: the input transistor was sized up by 20%. The goal of this change is to bias the transistor closer to threshold therefore get better g_m consequently better noise figure under the same bias current. The measurements indicate changes toward the opposite direction: the noise figure is worse, almost 0.5 dB higher, and the gain is lower by 1 dB. There are two possible reasons. First, while the increase of the input tran-

sistor size brings up g_m , it also increases the input capacitance consequently lowers the input Q . The final $g_m Q$ product may be lowered, which will result in worse noise figure and gain. Second, since the transceiver was fabricated in a different 0.25- μm run, the process variations may put the performance of the chip at worse case compared to stand-alone chip.

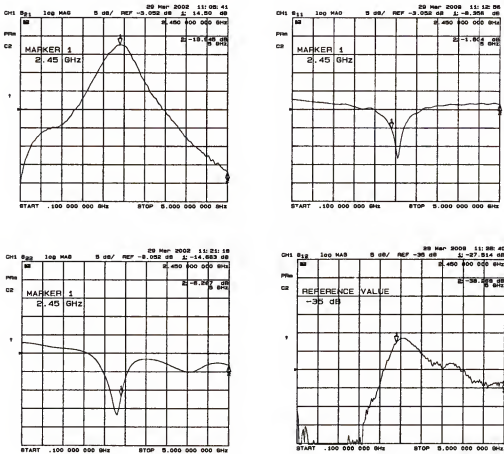


Figure 8-3 LNA S-parameters

The LNA is measured at a V_{DD} of 3V. Figs. 8-3 and 8-4 show the S-parameters and Noise Figure of the LNA. For 9 mA current, the transducer gain (S_{21}) is around 14.5 dB. Transducer gain changes less than 0.1 dB when V_{DD} changes from 3.3 V to 2.7 V.

Digital circuits do not affect LNA gain either. Turning on frequency synthesizer does not affect the LNA s-parameters. However, it *does* affect the Noise Figure of the LNA. NF is increased from 3.3 dB to 3.5 dB when synthesizer is on.

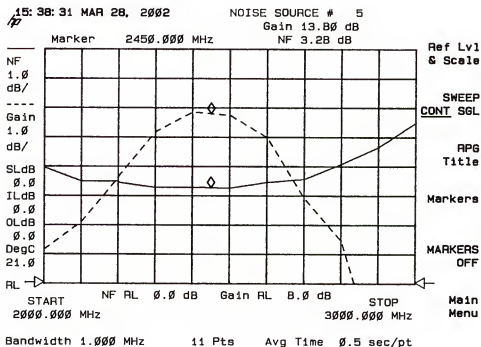


Figure 8-4 LNA Noise Figure

Table 8-1 LNA Performance Comparison

$f_0 = 2.45$ GHz	LNA in CMOS TRx	Stand-alone CMOS LNA	SiGe LNA
50- Ω NF	3.28 dB	2.88 dB	2.86 dB
Bias Current	9 mA	8.1 mA	7.0 mA
Transducer Gain	14.5 dB	15.1 dB	15.9 dB
S_{11}	-8.3 dB	-14.2 dB	-12.7 dB
S_{22}	-14.7 dB	-20.2 dB	-16.0 dB
S_{12}	< -27	< -34	< -30
IIP ₃	0.3 dBm	2.2 dBm	-2.6 dBm
IP _{1dB}	-8.5 dBm	-7.0 dBm	-11.2 dBm
Input transistor size	500 μ m/0.24 μ m	400 μ m/ 0.24 μ m	Not Appl.

Table 8-1 compares the LNA in the CMOS transceiver with previously built stand-alone CMOS LNA and the SiGe LNA. The change of the input transistor size has deteriorated the LNA performance in every category.

8.1.2 Rx Mixer Measurement Results

The RMx of CMOS TRx was also based upon the previously built stand-alone RMx. The transistor size, load are the same for the two. One adjustment made on RMx (part of the TRx), as shown in Fig. 8-5, is that the common mode inductor was replaced by an nMOS current source. From a system point of view, the large common mode inductor is prone to picking up low frequency noise from the substrate.

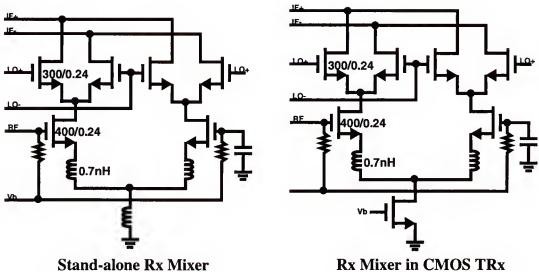


Figure 8-5 Two Rx mixers

Compared to stand-alone RMx, there is one big difference in measurement for the RMx in TRx: the LO frequency is set by the on-chip synthesizer now. The bias conditions for the two are very similar though, total RMx current is 16.1 mA, of which 12 mA is consumed by switching core, 4 mA by source follower and LO driver (this is close to 16 mA in simulation); LO diff/single end converter plus prescaler buffer consumes 9.6 mA (this is

3 mA more than 6.5 mA in simulation); prescaler 6.5 mA (this is close to 6 mA in simulation). Charge pump 1 mA, same as simulation. The performance of this RMx is worse than the previous built stand-alone RMx. The RMx exhibits a gain of 5.6 dB, 2.4 dB lower than the stand-alone RMx. The reason is that, now the LO is generated from the VCO instead of a signal source, the VCO has fixed output power resulting in LO input power around -6 dBm; where in stand-alone RMx measurement this LO can be adjusted to higher LO power, -3 dBm or higher, which helps to boost the CMOS mixer gain. Process variations may also bring some performance deterioration.

Fig. 8-6 and 8-7 show the input and output matching as well as the DSB Noise Figure of the RMx. S_{11} , the RF input, is matched at 2.4 to 2.5 GHz; S_{22} , the IF output, is matched at 375 MHz. Both input and output are well matched (less than -10 dB). The DSB Noise Figure is 8.2 dB, which translates to a SSB NF around 11.2 dB. That is close to the previous stand-alone RMx NF. Table 8-2 compares the performance of three mixers, the RMx in TRx, stand-alone RMx and the SiGe RMx.

Table 8-2 Rx Mixer Performance Comparison

	RMx in CMOS TRx	Stand-alone CMOS RMx	SiGe RMx
Power Gain	5.6 dB	8.0 dB	8.1 dB
SSB Noise Figure	11.2 dB	10.5 dB	9.0 dB
RF input and IF output matching	< -10 dB	< -10 dB	< -10 dB
Core Current	12 mA	12 mA	10 mA
IIP ₃	2.0 dBm	3.0 dBm	6.2 dBm
IP _{1dB}	-8.0 dBm	-6.0 dBm	-3.1 dBm
LO to IF feedthrough	-46 dB	-32 dB	-40 dB
RF to IF feedthrough	-12 dB	-14 dB	Not Avail.

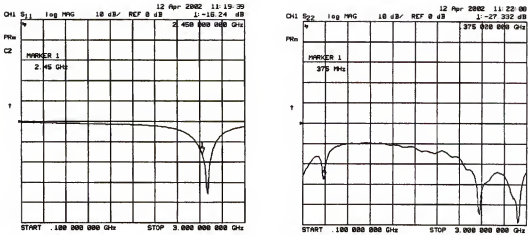


Figure 8-6 RMx input (RF) and output (IF) matching

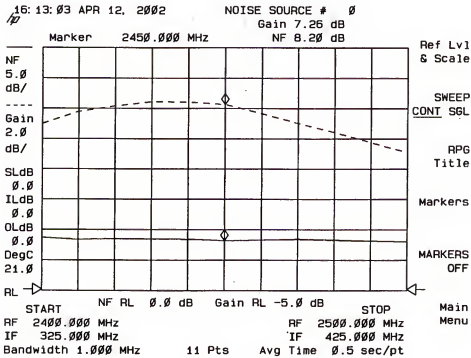


Figure 8-7 RMx Noise Figure

8.1.3 CMOS TRx Receiver Chain Measurement Results

As it turned out in PRISM II.5 system design, generally, the image rejection filter after the LNA is not needed. In PRISM II.5 WLAN reference design, the LNA output and Rx Mixer input are connected directly through a 50 Ω line on the PC board. On the RF transceiver evaluation board, inputs and outputs of the LNA and RMx are all connected to SMA connectors. Therefore the receiver can be measured by hooking up the LNA output SMA and Rx mixer input SMA directly using a semi-rigid cable.

The receiver is measured with a V_{DD} of 3V. The LO frequency is set by the on-chip synthesizer. The total current while the TRx is in Rx mode, is 69 mA, of which 27 mA is consumed by off-chip components (VCO, crystal oscillator, etc.). The RF signal is at 2.455 GHz and LO is at 2.08 GHz resulting the IF at 375 MHz. Figure 8-8 shows the receiver IF output signal seen on a spectrum analyzer. With the RF input at -40 dBm, the Rx chain exhibits a power gain of 18.7 dB.

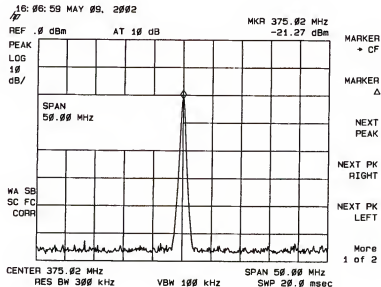


Figure 8-8 Receiver output

Fig. 8-9 shows a wider spectra of the receiver output. The LO signal is at -51 dBm, a rejection of 45 dB; RF signal is at -37.5 dBm, a gain of 2.5 dB; the signal at 1.705 GHz is the result of mixing RF and 2 LO, $2 \text{ LO} - \text{RF} = 1.705 \text{ GHz}$, it's at -58 dBm.

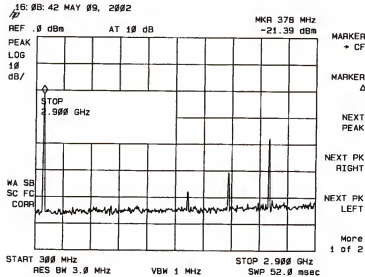


Figure 8-9 Rx output spectra

Due to the tuned response of LNA and RMx, the receiver will provide some image rejection. Fig. 8-10 is the spectrum at IF output when the RF input is at image frequency, 1.705 GHz, with a power of -40 dBm. The output is at the same 375 MHz IF, the output power is -38.5 dBm, demonstrating that the Rx chain has gain of 1.5 dB at image frequency. It's 17 dB less than the signal gain (which will have small impact on noise figure), or exhibits 17 dB image rejection, bringing more image rejection besides the 45 dB rejection from the front-end bandpass filter or additional image rejection filter.

Fig. 8-11 shows the single side-band (SSB) noise figure of the receiver. The receiver has a SSB noise figure of 5.1 dB. During the measurement, a bandpass filter was placed in front of the Rx. The filter has 1.2 dB loss at the signal frequency, and more than

40 dB rejection at the image frequency. Figs. 8-12 and 8-13 show the P_{1dB} and IP_3 plots of the receiver.

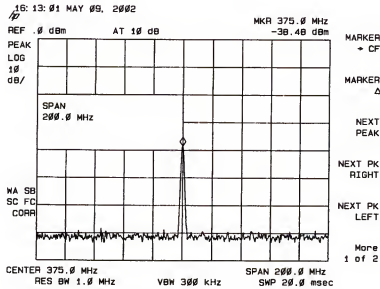


Figure 8-10 Receiver output when RF is at the image frequency

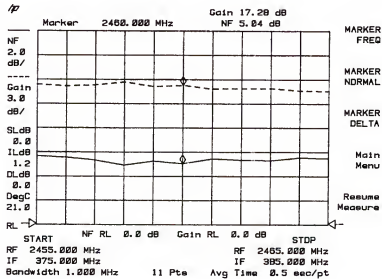


Figure 8-11 Rx chain noise figure

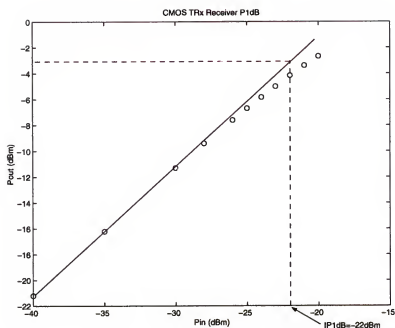
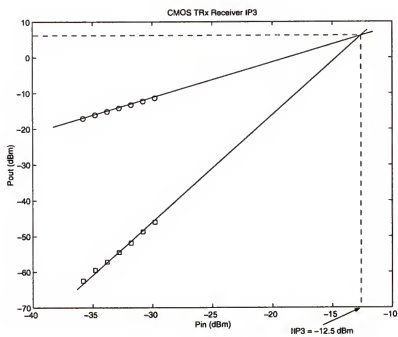
Figure 8-12 CMOS Rx P_{1dB} Figure 8-13 CMOS Rx IP_3

Table 8-3 tabulates the CMOS and SiGe Rx chain performance. CMOS receiver has 6 dB lower gain (3dB less each from LNA and mixer) and 1.5 dB worse noise figure. The IIP_3 and IP_{1dB} of the two receivers are close. The total receiver current for CMOS transceiver is 42 mA, including current consumption of LNA, synthesizer, LO buffer and RMx, excluding power consumption by all the off-chip components, it is 10 mA more than its SiGe counterpart.

Table 8-3 Receiver Performance Comparison

	CMOS Rx	SiGe Rx
Power Gain	18.7 dB	25 dB
Power Gain at Image	1.5 dB	Not Avail.
Image Rejection (No Filter)	-17.2 dBc	-14 dBc
Noise Figure	5.1 dB (SSB)	3.7 dB (SSB)
RF input and IF output matching	< -10 dB	< -10 dB
Input IP_3	-12.5 dBm	-12 dBm
Input P_{1dB}	-22 dBm	-23 dBm
LO to IF feedthrough	-45 dB	Not Avail.
RF to IF feedthrough	2.5 dB	Not Avail.
Total Rx Current *	42 mA	32 mA

* Including LNA, Synthesizer, LO Buffer and RMx, excluding power consumption by all the off-chip components.

8.1.4 Tx Amplifier Measurement Results

Fig. 8-14 shows the schematic of CMOS and SiGe TXA's. The CMOS TXA assumes a single stage, common source cascode configuration and the SiGe TXA is a simple one transistor common emitter amplifier. Usually the noise figure is not a huge concern in transmitter design so both TXA's are matched with an on-chip inductor at the input. The gain and linearity of TXA is much lower than simulation.

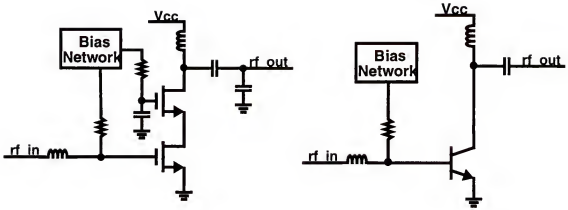


Figure 8-14 CMOS (Left) and SiGe (Right) Transmit amplifiers

The TXA small signal S-parameters are shown in Fig. 8-15. The total current of the TXA is 16 mA, small signal gain is 13.7 dB, 6.2 dB below simulation. Once the current increases to a certain point, (when MOSFET's are biased into strong inversion) further increasing current does not increase g_m or gain: at 18 mA the gain is 14.1 dB while at 20 mA the gain 14.6 dB, only less than 1 dB increase compared to 16 mA bias. Table 8-4 compares the CMOS TXA measurement results to simulation as well as those of SiGe TXA. The disparity between simulation and measurement is large in CMOS TXA, for both gain and linearity. The possible reasons are: first, the modeling of MOSFET transistor is not accurate at the RF frequencies, g_m/I_d decreases as the device is driven further into strong inversion. Probably a larger device should be employed to realize large gain in single stage CMOS amplifier. Second, the on-chip input matching inductor may be lossier than modeled in simulation.

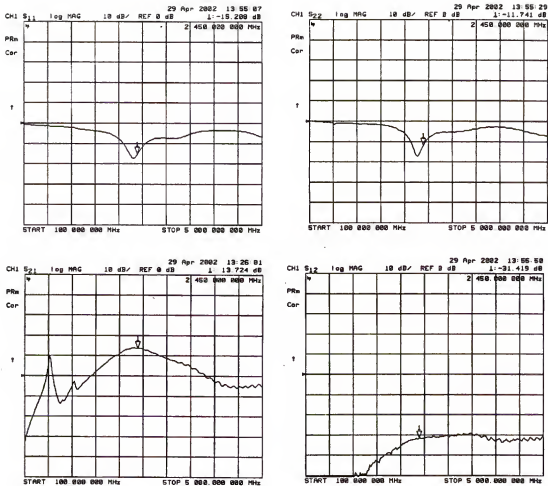


Figure 8-15 TXA Small Signal S-parameters

Table 8-4 Tx Amplifier Performance Comparison

	CMOS TXA Measurement	CMOS TXA simulation	SiGe TXA
Power Gain	13.7 dB	19.9 dB	16.7 dB
Input and output matching	< -10 dB	< -10 dB	< -10 dB
Core Current	16 mA	16 mA	15 mA
OIP ₃	9.0 dBm	16.0 dBm	Not Avail.
OP _{1dB}	2.0 dBm	6.0 dBm	7.0 dBm

8.1.5 Tx Mixer Measurement Results

The output of the Tx mixer (TMx) is matched on-chip to $50\ \Omega$. The input of TMx shares the same matching network as the output of the RMx because the IF SAW filter is shared by both Rx and Tx chains. The LO frequency is set by the on-chip synthesizer running at 2.082 GHz. The IF input is -30 dBm at 375 MHz. The RF output is measured to be -26.5 dBm at 2.457 GHz as shown in Fig. 8-16. The TMx exhibits a gain of 3.5 dB, 1.5 dB lower than simulation. Fig. 8-17 shows the TMx RF output matching.

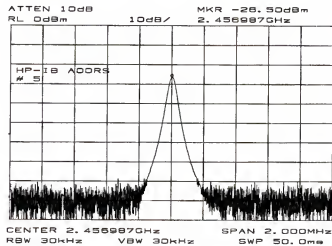


Figure 8-16 TMx output spectrum

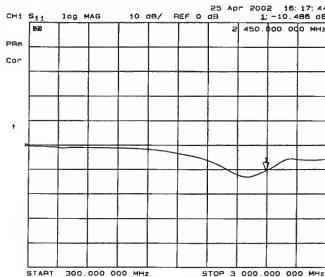


Figure 8-17 TMx RF output matching

Figs. 8-18 and 8-19 show the IP_3 and P_{1dB} measurements at the mixer output.

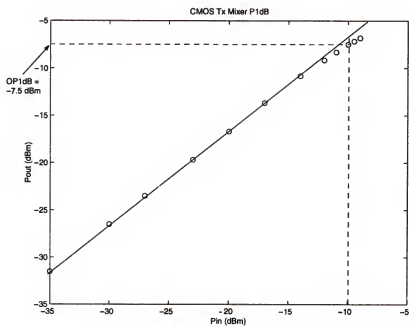


Figure 8-18 TMx P_{1dB}

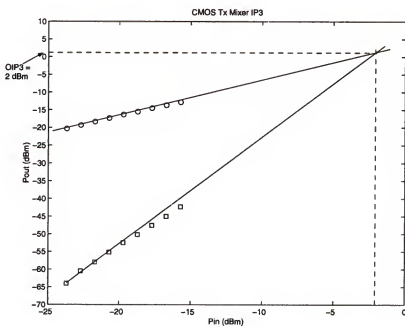


Figure 8-19 TMx IP_3

Table 8-5 shows the comparison of CMOS and SiGe TMx. CMOS mixer demonstrates good IF-RF feedthrough, < -45 dB. LO to RF feedthrough is -28 dB. The image output (at 1.7 GHz) has -2 dB gain. The total current of TMx is 23 mA, of which 17.5 mA is consumed by the mixer core, 5.5 mA by the source follower and LO driver (this is 2.5 mA more than a total of 20.5 mA in simulation); LO diff/single-end converter plus prescaler buffer consumes 11.6 mA (this is 5 mA more than 6.5 mA in simulation); prescaler 6.5 mA (this is close to 6 mA in simulation); charge pump 1 mA, the same as simulation.

Table 8-5 Tx Mixer Performance Comparison

	CMOS TMx	CMOS TMx simulation	SiGe TMx
Power Gain	3.5 dB	5 dB	9 dB
IF input and RF output matching	< -10 dB	< -10 dB	< -10 dB
Core Current	17.5 mA	16 mA	10 mA
OIP ₃	+2.0 dBm	+3.0 dBm	Not Avail.
OP _{1dB}	-7.5 dBm	-5.5 dBm	-6 dBm
LO to RF feedthrough	-28 dB	-33 dB	Not Avail.
IF to RF feedthrough	< -45 dB	-41 dB	Not Avail.

8.1.6 CMOS TRx Transmitter Chain Measurement Results

Same as in the receiver measurements, the transmitter is formed by connecting Tx Mixer output and TXA input directly off-chip using a semi-rigid cable on the RF/IF converter evaluation board. At V_{DD} of 3V, the Tx chain of the CMOS transceiver consumes 55 mA. The IF is at 375 MHz and LO is at 2.08 GHz resulting an RF signal at 2.455 GHz. Figure 8-20 shows the measured RF output spectrum, with the IF input at -35 dBm. The Tx chain exhibits power gain of 17.5 dB. Figure 8-21 shows a wider spectrum of the RF

output, various spurious components can be seen. The LO signal experienced a rejection of 30 dB; IF signal is less than -70 dBm, a rejection of more than 35 dB.

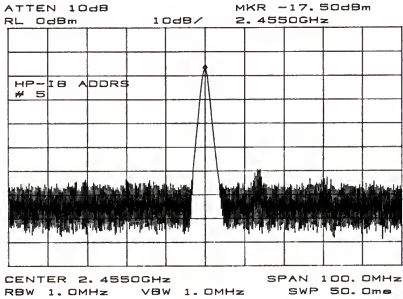


Figure 8-20 Tx signal output

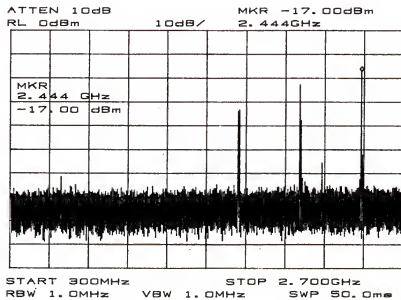


Figure 8-21 Tx output spectra

Fig. 8-22 shows the RF output spectrum at 1.705 GHz, where the image frequency ($LO - IF$) is located. With IF input of -35 dBm, the Tx has gain of 1.7 dB at image frequency. A 15 dB (17.5 dB - 1.7 dB) image rejection is obtained due to the tuned response.

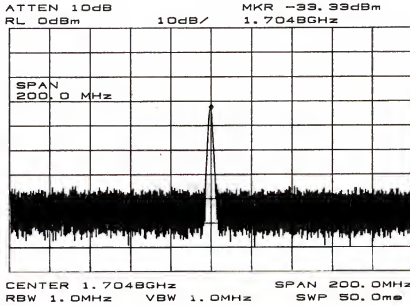


Figure 8-22 Tx image output

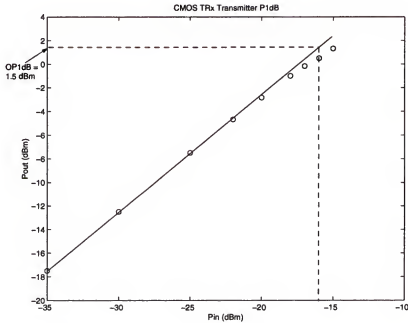


Figure 8-23 CMOS Tx P_{1dB}

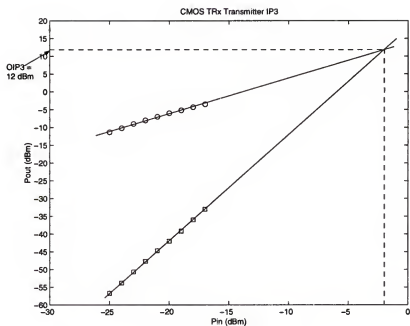
Figure 8-24 CMOS Tx IP₃

Table 8-6 Transmitter Performance Comparison

	CMOS Tx	SiGe Tx
Power Gain	17.5 dB	25 dB
Power Gain at Image	1.7 dB	Not Avail.
Image Rejection	-15.8 dBc	Not Avail.
IF input and RF output matching	< -10 dB	< -10 dB
Output IP ₃	12 dBm	14 dBm
Output P _{1dB}	1.5 dBm	4 dBm
LO to RF feedthrough	-30 dB	-25 dB
IF to RF feedthrough	< -35 dB	Not Avail.
Total Tx Current	55 mA	41 mA

Fig. 8-23 and 24 are the Tx IP₃ and P_{1dB} plots. Notice that in the Tx, these specs are defined at the output instead of the input. Table 8-6 compares the performance of the CMOS and SiGe Tx chain. The power gain of the CMOS Tx is 7.5 dB lower than that of

the SiGe Tx. The lower power gain will limit the CMOS radio total Tx output power if the PA cannot compensate missed gain.

8.2 Summary of CMOS RF Transceiver Design and Measurement

The design of the CMOS RF transceiver is successful with all the blocks on the chip functioning well. However, the overall performance of the transceiver is not as good as expected. On the receiver side, LNA and RMx performance is slightly worse than the previous built stand-alone ones. Although process variations could explain some of the performance difference. Some design issues like the re-size of the LNA and on-chip synthesizer generated LO are part of the reason as well. On the transmitter side, the disparity between the performance of measured and simulated TMx and TXA is relatively large. The main reason is the modeling accuracy for RF CMOS devices. The models used for simulation are the foundry provided BSIM models for digital applications. The proper modeling of the RF devices has become increasingly important as RF CMOS strives to compete with Si or SiGe BiCMOS processes.

Table 8-7 Comparison of 0.18- μm and 0.25- μm CMOS processes

Parameters	0.18- μm CMOS	0.25- μm CMOS
Peak f_T (GHz)	55	40
g_m/I_d ratio (V^{-1})	30	15
NF_{\min} (dB)	1.2	1.4

The technology scaling will certainly help the cause of RF CMOS. Compared to the 50 GHz SiGe BiCMOS process used for the SiGe transceiver, the 0.25- μm CMOS is still much slower. Moving to 0.18- μm will bring speed parity to the SiGe BiCMOS process. Table 8-7 compares the 0.18- μm and 0.25- μm CMOS technology [Abo00, Che01]. The benefit of speed and noise is obvious. On top of that, for 2.4GHz applications, the

speed of 0.18- μm CMOS process leaves room for better process variations (discussed in chapter 4) and hot-electron reliability if the RF device is designed with gate length larger than the minimum. As the 0.18- μm CMOS becomes main stream digital process, its wafer price will start to drop. All these will give competitive edge to CMOS process for 2.4 GHz applications.

8.3 CMOS TRx In PRISM II.5 Radio

8.3.1 Introduction

As an ultimate evaluation of CMOS transceiver and the comparison between BJT and CMOS RF circuits, the CMOS transceiver part has been measured in a PRISM radio.

8.3.2 Measurement Setup

Two laptops are used in the setup, one acting as a radio transmitter, the other as a receiver. A radio link is established between them. The Tx is shielded in a metal box, attenuators are mounted on the box to control the Tx output power. An external signal generator produces the jammer signals. Two software, LANEVAL and Prism Test Utility, are used for radio evaluation.

Unlike the chip level testing, where specifications like S-parameters, Noise Figure, linearity are measured, for 802.11b WLAN system (a packet radio system) testing, Packet Error Rate (PER) is used as criterion to measure the radios. Two PRISM II.5 cards are used to benchmark the SiGe radio. Specifications like Rx sensitivity, image rejection, adjacent channel rejection; Tx spectral mask, output RMS power are measured.

8.3.3 CMOS Radio Setup

To measure the CMOS radio, SiGe TRx chip on one PRISM II.5 card was detached or bypassed. Shown in Fig. 8-25, an impedance transformer (1:4) was mounted

on the board right after the SAW filter (which has $200\ \Omega$ differential impedance) and a coaxial probe with SMA connector was soldered to the transformer. Two more coaxial probes with SMA connector are soldered on the board: one connected to the Tx chain and goes into the PA, and the other connected to the Rx chain and routed out of the front-end band pass filter.

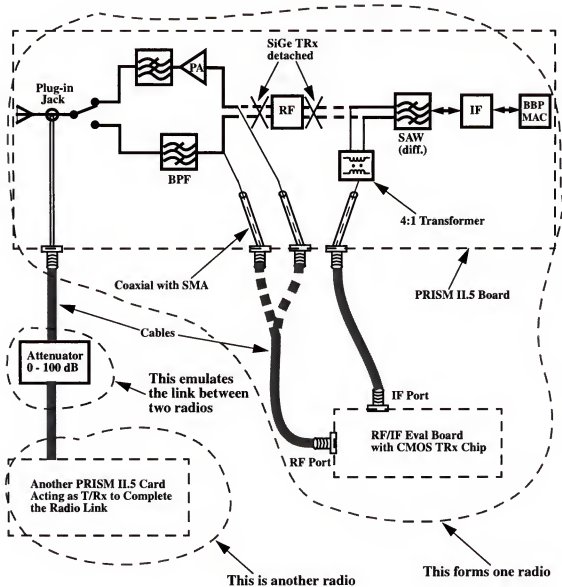


Figure 8-25 Radio measurement setup

8.3.4 Transmitter Measurement Results

During the measurements, the radio with CMOS TRx transmits 1000 byte packets at 11Mbps. The signal is fed into a Tektronix Wireless Communication Analyzer where constellation, EVM and eye pattern are measured. The original PRISM II.5 (SiGe TRx) signals are also measured for comparison.

Fig. 8-26 shows the EVM measurement of CMOS and SiGe transmitters.

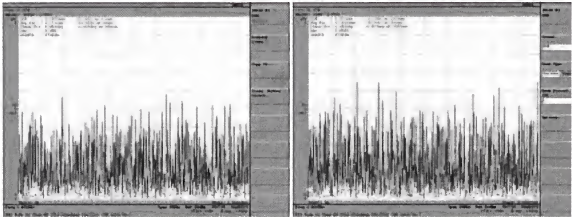


Figure 8-26 Left, EVM of radio transmitter with a CMOS TRx, ~ 5.3%, around -25.5 dB; Right, EVM of PRISM II.5 radio transmitter with a SiGe TRx, ~ 5.3%, around -25.5 dB.

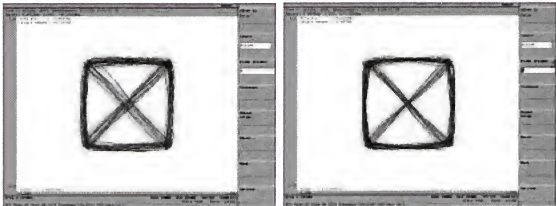


Figure 8-27 Left, Constellation diagram of radio transmitter with a CMOS TRx; Right, Constellation diagram of PRISM II.5 radio transmitter with a SiGe TRx.

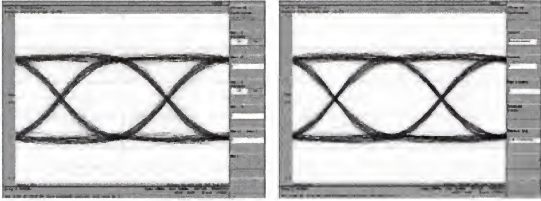


Figure 8-28 Left, Eye Pattern of radio transmitter with a CMOS TRx; Right, Eye Pattern of PRISM II.5 radio transmitter with a SiGe TRx.

Figures 8-27 and 8-28 demonstrate the constellations and eye patterns of the transmitted signal. The Prism Test Utility software can program the Tx to transmit continuous wave signals. The output spectrum can be seen on a spectrum analyzer. Shown in Fig. 8-29 is the transmit output spectra of the two radios. Fig. 8-30 demonstrates the Adjacent Channel Power Ratio (ACPR) or the spectral mask of the transmitted signal of both radios.

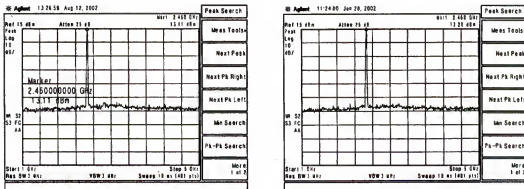


Figure 8-29 Left, output spectrum of Radio Transmitter with a CMOS TRx, output power 13.1 dBm; Right, output spectrum of PRISM II.5 Radio Transmitter with a SiGe TRx, output power 13.2 dBm.

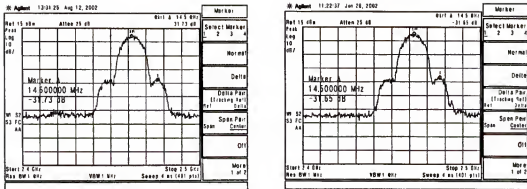


Figure 8-30 Left, spectrum mask of radio transmitter with a CMOS TRx, ACPR first sidelobe -31.7 dBc; Right, spectrum mask of PRISM II.5 radio transmitter with a SiGe TRx, ACPR first sidelobe -31.7 dBc.

The transmitter performance of CMOS and SiGe radios is very close if not identical. Yet from RF measurement, the CMOS TRx fares much worse than SiGe TRx. The total gain of the transmitter chain is almost 8 dB less while the compression points are also 2.5 dB worse. This radio level parity can be attributed to the robustness of superheterodyne system design as well as the high performance PA. The PA has a small signal gain of 26 dB and 1dB compression point of 18 dBm. To meet the ACPR linearity requirement, the PA output backs off 3 dB from its compression point, i.e., 15 dBm. Through Tx Automatic Gain Control (AGC), that roughly puts the output power of the transmitter around -10 dBm, way below either CMOS and SiGe Tx output compression point. Therefore the ACPR of two radios is close. Also, the IF transmitter is designed to leave large margin for maximum gain and dynamic range. The Tx AGC will control the IF transmitter to compensate the less gain in CMOS Tx. Consequently the output power of the two radios is very close as well.

8.3.5 Receiver Measurement Results

Packet Error Rate (PER) is the criterion to evaluate the performance of a packet radio like 802.11b radios. LANEVAL program can calculate PER when the radio is in the receiving mode. As shown in Fig. 8-25, during the measurement, one PRISM II.5 card transmits at 11 Mbps at full power, the signal is routed through attenuators where the attenuation ranges from 0 to 120 dB. The attenuated signal goes into the antenna of the receiver radio (with CMOS TRx). Through monitoring PER at different signal levels, specifications like sensitivity, image rejection, adjacent channel rejection can be measured. Usually for one PER measurement, 10,000 packets are counted and their PER is averaged. Generally, if the PER is above 8%, the radio is considered out of reception. Fig. 8-31 shows the measured receiver sensitivity of the two WLAN radios at 11 Mbps data rate. The CMOS and SiGe radios have Rx sensitivity of -81 dBm and -84 dBm respectively. Both of them are much better than the -76 dBm required by the 802.11b standard.

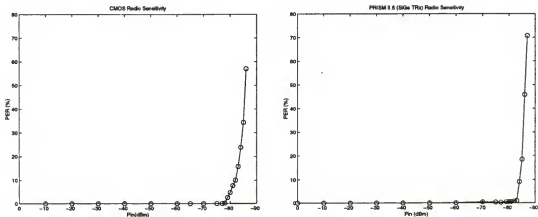


Figure 8-31 Left, CMOS radio sensitivity, @ 11 Mbps, -81 dBm; Right, PRISM II.5 SiGe radio sensitivity, @ 11 Mbps, -84 dBm.

Adjacent channel rejection is tested with a 25-MHz separation between channels. The desired channel input power is set to be -78 dBm for the CMOS radio, -80 dBm for

the SiGe radio, (@2.462 GHz, channel 11). The input power is chosen to be 3 dB higher than the sensitivity level to ensure that the radios are in good reception (no residual PER) before the jammer signals are applied. The PER of the radios is measured while varying the power of CW on the adjacent channel. The jammer on adjacent channel (@2.437 GHz) is 11 Mbps CCK modulated signal in CW form. An Arbitrary Wave Form generator generates the I & Q channel CCK baseband signals. The I & Q signals are then up-converted to signal at the adjacent channel through vector modulation using a Rhode & Schwartz signal generator. Fig. 8-32 shows the receiver adjacent channel rejection performance of the CMOS and SiGe radios. The PER is larger than 8% when the adjacent channel power exceeds -30 dBm for both radios. This gives the image rejection of (-30 dBm) - (-78 dBm) = 48 dBc, and (-30 dBm) - (-80 dBm) = 50 dBc for CMOS and SiGe radios, respectively.

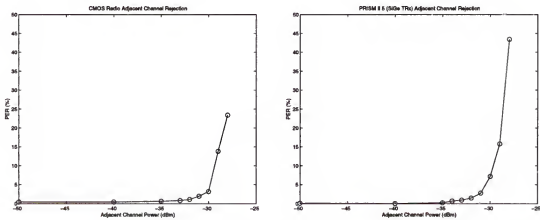


Figure 8-32 Adjacent channel rejection: Left, CMOS radio adjacent channel rejection, (-30 dBm) - (-78 dBm) = 48 dBc; Right, PRISM II.5 radio adjacent channel rejection, (-30 dBm) - (-80 dBm) = 50 dBc.

For image rejection test, again, the desired channel input power is set to be -78 dBm for the CMOS radio, -80 dBm for the SiGe radio. The image is generated at $RF - 2 IF = 2.462 \text{ GHz} - 2 \times 374 \text{ MHz} = 1.714 \text{ GHz}$ for channel 11 (2.462 GHz). The PER of the

radios is measured while varying the power of CW at image frequency. Fig. 8-33 shows the receiver image rejection performance of the two radios. The PER is larger than 8% when the image power exceeds -17 dBm and -27 dBm, resulting in image rejection of 61 dB and 53 dB for CMOS and SiGe radios respectively.

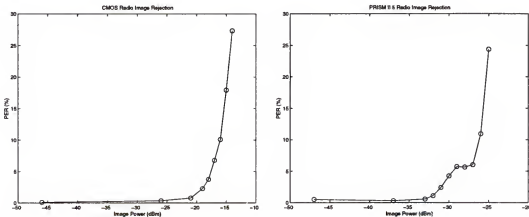


Figure 8-33 Receiver image rejection: Left, CMOS radio image rejection, (-17 dBm) - (-78 dBm) = 61 dB; Right, PRISM II.5 radio image rejection, (-27 dBm) - (-80 dBm) = 53 dB.

Table 8-7 summarizes and compares the performance of the PRISM II radio with a CMOS transceiver chip and the radio with SiGe transceiver chip.

Table 8-8 Radio (802.11b) Performance Comparison

	CMOS Radio	PRISM II.5 (SiGe) Radio
Rx Sensitivity (11 Mbps, 8% PER)	-81 dBm	-84 dBm
Rx Image Rejection	61 dB	53 dB
Rx Adjacent Channel Rejection	48 dBc	50 dBc
Tx Output Power	13.1 dBm	13.2 dBm
Tx Output Spectral Mask (1st sidelobe)	-31.7 dBc	-31.7 dBc
Tx Output EVM	-25.5 dB	-25.5 dB

8.4. Summary of the Characterization of CMOS Transceiver

A CMOS RF transceiver for 802.11b WLAN application is designed in a 0.25- μm CMOS technology. The CMOS transceiver is incorporated in a WLAN system and its radio performance is evaluated. The performance of the two radios is close due to the robustness of superheterodyne radio design. The CMOS transceiver has slightly higher noise figure and lower power gain than the SiGe one. The loop bandwidth of the PLL frequency synthesizer is set to be 1 kHz. Phase noises of the CMOS and SiGe PLL synthesizers are -81 dBc/Hz and -83 dBc/Hz at 10 kHz offset, respectively. The total current consumption of CMOS transceivers is 10 mA (in the Rx mode) and 15 mA (in the Tx mode) more than its SiGe counterpart. When the power consumption of the entire radio is considered, CMOS radio consumes less than 5% more current than that for the SiGe radio. The -81 dBm CMOS receiver sensitivity is 5 dB better than what's required by the IEEE 802.11b standard. Moving to a 0.18- μm CMOS technology will most likely bring CMOS chip RF performance close to or exceed that of the SiGe chip. The results suggest it should be possible to replace the SiGe transceiver with low cost CMOS transceivers and "RF CMOS" is viable in delivering 2.4 GHz WLAN chip-set solution.

CHAPTER 9 SUMMARY AND FUTURE WORK

9.1 Summary

The first part of the dissertation studied the feasibility and difficulty of implementing a CMOS transceiver by building and testing individual blocks. Stand-alone CMOS LNA and Rx mixer were first built and the silicon measurement results were compared with their SiGe counterparts. The comparison indicates that CMOS blocks are able to meet the RF specifications of the receiver. CMOS transistors are adequate in building RF amplifiers and mixers with decent noise figure and power consumption for WLAN applications. The comparison of CMOS and SiGe LNA and mixer was summarized in [Li01]. Next, a stand-alone CMOS frequency synthesizer was designed. Measurements showed that the synthesizer works well and achieves comparable performance as its SiGe counterpart.

Based on the success of these individual blocks, the second part of the dissertation work focused on the realization of RF transceiver in CMOS. The chip was designed, fabricated, packaged and put on the PC board for evaluation. Measurements indicate an overall decent design with all the blocks functioning. The results were analyzed and compared to simulations as well as the SiGe chip results. One of the key results this chip provided is the impact of digital circuitry (Frequency synthesizer) on the performance of individual RF blocks (LNA, Mixers and TXA). This result can not be obtained in the study of individual blocks and will provide valuable guidance to future transceiver design. The mixers are

measured with LO set by the on-chip synthesizer. The output spectrum is clean and there is no significant degradation on noise figure due to the synthesizer. However, the LNA measurement indicates that turning on the synthesizer *does* affect the Noise Figure of the LNA. NF is increased from 3.3 dB to 3.5 dB when the synthesizer is on.

As an ultimate evaluation of the CMOS transceiver and the comparison between the SiGe BJT and CMOS RF circuits, the CMOS transceiver was incorporated in a PRISM radio and the whole WLAN system was evaluated. The IEEE 802.11b radio with a CMOS chip is successfully demonstrated. The performance of the CMOS and SiGe radios is close. This work has provided experimental results supporting the feasibility and competitiveness of CMOS technology for WLAN applications.

9.2 Future Work and Direction

The successful implementation of the CMOS transceiver and the robust demonstration of WLAN system with the CMOS chip opens the door for a higher level of integration. Within the same superheterodyne transceiver architecture, a few possible future works are suggested.

9.2.1 CMOS Transceiver with a T/R Switch

A CMOS Transceiver with T/R switch can be designed based upon [Hua01] and the CMOS transceiver presented in this dissertation. One natural issue arises when the T/R switch is placed on the same chip as the transceiver, that is, the interface between them. On a PC board where the T/R switch and TRx are in separate chips, for example, the PRISM II system in Fig. 9-1, the interface is 50 Ω .

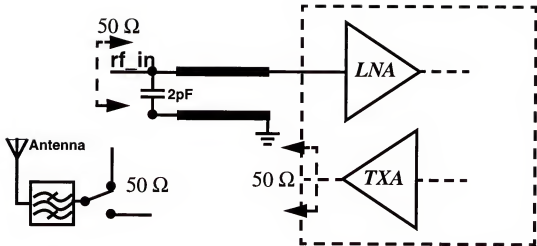


Figure 9-1 PRISM II RF transceiver and T/R switch interface

The situation could be different if the T/R switch and TRx are on the same chip. If the Single Pole Double Throw (SPDT) switch is integrated with the single pole connected to one pin which eventually leads to antenna, one throw for LNA and another throw for PA or TXA, the impedance of the interface between switch and LNA, or switch and TXA/PA, will not be $50\ \Omega$. This is because the LNA requires off-chip component for matching: a piece of transmission line and a shunt cap. (On-chip $50\ \Omega$ matching is not desirable as the on-chip inductor will degrade the LNA noise figure.)

A PA with more than 20 dBm output power is needed for general WLAN applications. This usually requires an off-chip PA. In this case, the interface between one throw of the SPST switch and PA output has to be $50\ \Omega$. A natural scheme to integrate the T/R switch with the TRx is to treat the T/R switch as a stand-alone circuit, shown in Fig. 9-2.

The CMOS T/R switch takes advantage of MOSFET being naturally a good switch. The design of a transceiver with an on-chip T/R switch will bring the state of the

art integration level into Wireless LAN transceiver design and demonstrate the unique advantage of “RF CMOS.”

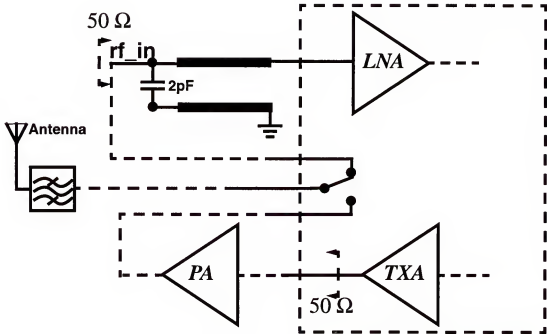


Figure 9-2 T/R switch interface

9.2.2 Transceiver with On-chip PA

An RF transceiver with an on-chip PA will further elevate the integration level and bring down the cost. It will also simplify the integration of the on-chip switch. One possible implementation is shown in Fig. 9-3. Since the T/R switch is supposed to have low insertion loss, the impedance added by the switch should be small. Therefore, the PA can be directly connected to one throw of the switch. The other throw of the switch can go off-chip to the LNA matching network. The single pole will eventually lead to the antenna. The LNA is still matched to 50 Ω when the receiver is switched on and the PA will see 50 Ω when the transmitter is switched on.

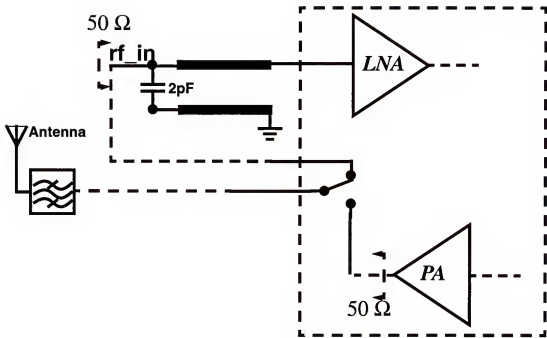


Figure 9-3 CMOS Transceiver with integrated PA and T/R switch

This system requires a good design on both the PA and T/R switch. The previous work shows a P_{1dB} of the on-chip T/R switch around 18 dBm without off-chip matching [Hua01]. This limits the total power out of the PA; consequently the entire radio transmit power which may not be acceptable for WLAN access point. However, this system may still be a viable low-cost WLAN solution for mobiles.

9.2.3 Transceiver with Integrated IF Transceiver

Another opportunity for integration is the IF section of the radio. There is no fundamental difficulty in doing so as all the circuits in the IF section are realizable in CMOS. The IF output of the RF transceiver can go off-chip to the SAW filter and come back to the IF section of the chip, as shown in Fig. 9-4.

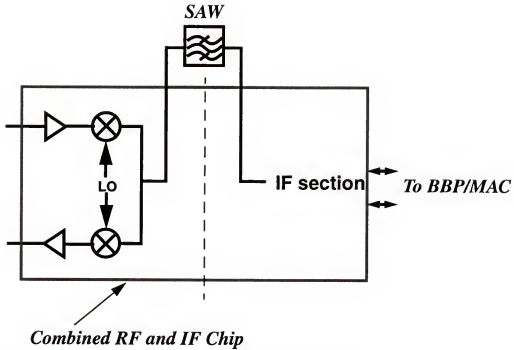


Figure 9-4 A chip integrating both RF and IF transceivers

The highest level of integration for a superheterodyne transceiver can be achieved by incorporating the concepts in Figs. 9-3 and 9-4. A CMOS chip integrating a PA, a T/R switch, RF and IF sections will demonstrate the ultimate power of “RF CMOS.”

APPENDIX A

BJT AND MOSFET DEVICE PHYSICS

The I-V characteristics of BJT's and MOSFET's are mathematically simple. The I-V characteristics of BJT's are exponential and those of MOSFET's are square law. There must be simple physics behind the simple exponential or square law. Most of the textbooks emphasize on how to quantitatively derive the I-V equation. A simple, preferably one-sentence answer to questions like "Why exponential?" or "Why square law?" is more desirable. This discussion reveals more physics than a lengthy mathematical derivation and compares two devices on a more fundamental level.

A.1 Why Does the BJT Have Exponential I-V Relation?

In an npn BJT, the minority diffusion current density can be expressed as,

$$J = qD \frac{dn}{dx} \quad (\text{A.1})$$

where D is the diffusion constant. $\frac{dn}{dx}$ is proportional to minority carrier concentration at the base depletion edge of base-emitter junction,

$$\frac{dn}{dx} \propto \frac{n(0)}{W} \quad (\text{A.2})$$

where W is the base width. The carrier concentration $n(0)$, or the number of carriers (per unit volume) in a semiconductor is determined by Density of States of the conduction band and the Fermi-Dirac distribution. In the case of minority carriers in silicon, they reduce to an exponential,

$$n(0) \propto \exp\left(-\frac{E}{kT}\right) = \exp\left(\frac{\Delta V}{(kT)/q}\right) . \quad (\text{A.3})$$

BJT current is dominated by minority diffusion current (A.1). Therefore I-V expression of BJT is

$$I \propto \exp\left(\frac{\Delta V}{(kT)/q}\right) \quad (\text{A.4})$$

which gives the one-sentence answer to “Why exponential?”: BJT’s exhibit exponential I-V characteristics because the number of minority carriers (consequently diffusion current) has an exponential relationship with respect to (energy) the junction voltage.

A.2 Why Does the MOSFET Have Square Law I-V Relation?

The conducting mechanism of a resistor (or conductor) is majority carriers drifting under electric field. MOSFET discussion is restricted to the strong inversion case because the square law does not apply in the sub-threshold or weak-inversion regions. MOSFET’s can not be viewed as voltage controlled conductors in sub-threshold or weak-inversion. In these regions, its conducting mechanism is minority carrier diffusion like that found in diodes or BJT’s.

The drift current density of majority carriers under electric field is

$$J = \sigma E = qn\mu E , \quad (\text{A.5})$$

where σ is the conductivity and μ is the mobility. The channel conductance (conductivity) which is proportional to the number of majority carriers, is controlled by the voltage on the gate. Beyond the threshold voltage, in strong inversion, the channel is like a metallic conductor. The semiconductor underneath the channel is shielded from further penetration of electric field by the metallic channel. Any voltage increase on the gate will be dropped

across the gate oxide. The relationship between number of carriers in the channel and the gate voltage is linear, same as that of an ideal capacitor,

$$\delta Q = C \cdot \delta V \quad \text{or} \quad Q = qn = C \cdot V_{GT} \quad (\text{A.6})$$

where V_{GT} is $(V_G - V_{th})$. Considering the effects of drain voltage,

$$n(y) \propto (V_{GT} - V_c(y)) \quad (\text{A.7})$$

where y is the direction from source ($y = 0$) to drain ($y = L$), and $V_c(y)$ is the voltage along the channel. Substituting Eq. (A.7) into Eq. (A.5) and remembering that electric field is the derivative of potential $E \propto \frac{d}{dy}V(y) \propto \frac{d}{dy}n(y)$,

$$J \propto n(y) \cdot \frac{d}{dy}n(y) . \quad (\text{A.8})$$

Integrating Eq. (A.7) along y direction yields,

$$J \cdot L \propto n_{source}^2 - n_{drain}^2 . \quad (\text{A.9})$$

In saturation $n_{drain}^2 = 0$, so

$$J \propto n_{source}^2 \propto V_{GT}^2 \quad \text{in saturation.} \quad (\text{A.10})$$

Eq. (A.10) is the MOSFET square law. It is the natural result of Eq. (A.6), which states that the conductivity is proportional to effective control voltage. The one-sentence answer to “Why square law?” is, MOSFET’s exhibit square law because it acts like an ideal capacitor where the channel (one side of the capacitor) is a conductor whose conductivity is proportional to control voltage.

A.3 Field Effect Transistor and Square Law

From the above discussion, the mechanism for a square law device is the linear relationship between gate control voltage and number of carriers in the channel. The physics behind this is that, once the MOSFET is turned on (strong inversion), the nature of its channel is metallic. A further voltage increase on the gate will be dropped across the gate and channel (gate oxide). The semiconductor underneath the channel is shielded from further penetration of electric field by the metallic channel. The existing of the threshold voltage, V_{th} , is a key measure when the metallic channel has been established. Below threshold voltage or in sub-threshold region, the voltage on the gate is dropped partially across the oxide, partially across the semiconductor underneath. In semiconductor, the relationship between the number of carriers and voltage drop is exponential. That is why in sub-threshold region, MOSFET's behave like BJT's.

In strong inversion, when the conduction and valence bands are bent down far enough that surface potential $\psi_s = 2 \psi_B$, the semiconductor is effectively shielded from further penetration of the electric field by the inversion layer. Even a very small increase in the band bending (corresponding to a very small increase in the depletion layer width) results in a very large increase in the charge density within the inversion layer. Beyond threshold voltage, in strong inversion, most of the increase in gate voltage will drop across the oxide, with a tiny little across semiconductor to supply "enough" carriers to satisfy Eq. (A.6). One instant conclusion is that, the number of carriers in a MOSFET channel (with respect to gate voltage) can never exceed the number of carriers in a semiconductor pn junction (with respect to voltage across the junction) because, the latter is the supply of the former. Therefore, g_m/I ratio of a MOSFET will always be lower than that of a BJT.

APPENDIX B INPUT IMPEDANCE OF BJT AND MOS LNA'S

During the analyses of both BJT and MOS LNA's, the input impedance of cascode LNA's with inductive degeneration was needed. For example, the input stage of a cascode BJT LNA can be represented as Fig. B-1.

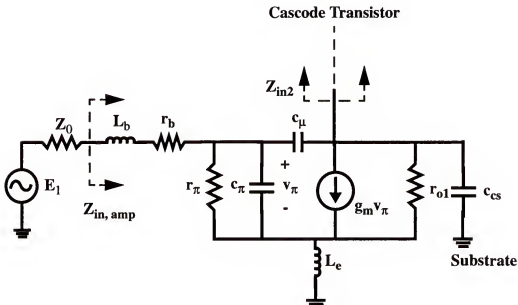


Figure B-1 Small signal representation of a BJT Cascode LNA input

The MOSFET LNA has the similar small signal model only simpler: r_g (r_b) can be neglected and r_π is infinite. The above model can be further generalized and simplified as Fig. B-2. In analyzing the input impedance, Z_b can be absorbed into Z_0 and the input impedance calculation is reduced to finding the input impedance of the circuit in Fig. B-3.

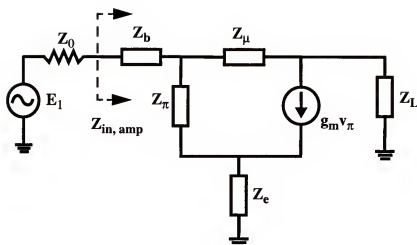


Figure B-2 General small signal model of a BJT LNA

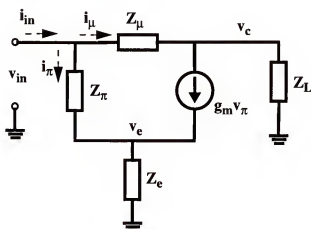


Figure B-3 Generic small signal model for input impedance calculation

B.1 Input Impedance of A Transistor with Degeneration

The precise expression of the input impedance for the circuit in Fig. B-3, a transistor with degeneration is calculated and presented here. Fig. B-3 is redrawn as Fig. B-4 where it can represent both BJT and MOS LNA's as well as a broad range of amplifiers fabricated with other active devices.

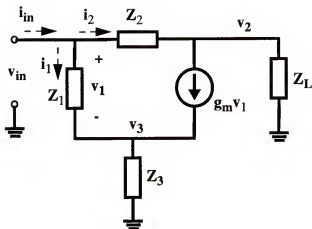


Figure B-4 Generalized small signal model of a transistor with degeneration

Using KVL and KCL, the basic equations are

$$i_{in} = i_1 + i_2, \quad (\text{B.1})$$

$$v_{in} = v_1 + v_3, \quad (\text{B.2})$$

where v_1 and v_3 are

$$v_1 = i_1 \cdot Z_1, \quad (\text{B.3})$$

$$v_3 = (i_1 + g_m v_1) \cdot Z_3. \quad (\text{B.4})$$

In addition,

$$v_{in} = v_1 + v_2, \quad (\text{B.5})$$

where v_2 can be expressed as

$$v_2 = (i_2 - g_m v_1) \cdot Z_L. \quad (\text{B.6})$$

Substituting Eqs. (B.3) and (B.4) into (B.2),

$$v_{in} = i_1 \cdot Z_a \quad (\text{B.7})$$

where Z_a is

$$Z_a = Z_1 + (1 + g_m Z_1) \cdot Z_3 \quad . \quad (B.8)$$

Substituting Eqs. (B.3) and (B.6) into (B.5),

$$v_{in} = i_2 \cdot (Z_2 + Z_L) - i_1 g_m Z_1 Z_L \quad . \quad (B.9)$$

For three equations (B.1), (B.7) and (B.9), there are four unknowns, v_{in} , i_{in} , i_1 and i_2 . These three equations can be solved to obtain i_{in} in terms of v_{in} consequently the input impedance Z_{in} .

Re-writing (B.7),

$$i_1 = \frac{v_{in}}{Z_a} \quad . \quad (B.10)$$

Substituting (B.10) into (B.9),

$$v_{in} = i_2 \cdot (Z_2 + Z_L) - \frac{v_{in}}{Z_a} g_m Z_1 Z_L \quad , \quad (B.11)$$

or

$$i_2 = \frac{v_{in}}{Z_2 + Z_L} \cdot \left(1 + \frac{g_m Z_1 Z_L}{Z_a} \right) \quad . \quad (B.12)$$

Substituting Eqs. (B.10) and (B.12) into (B.1),

$$i_{in} = v_{in} \cdot \left(\frac{1}{Z_a} + \frac{Z_a + g_m Z_1 Z_L}{Z_a \cdot (Z_2 + Z_L)} \right) \quad (B.13)$$

or

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{Z_a \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_a + g_m Z_1 Z_L} \quad (B.14)$$

where Z_a is

$$Z_a = Z_1 + (1 + g_m Z_1) \cdot Z_3 \quad (\text{B.15})$$

Equation (B.14) is the exact solution of the input impedance of a transistor with degeneration.

B.2 Approximation Cases

In several scenarios, including the LNA cases, approximation can be applied and Eq. (B.14) can be reduced into some familiar equations.

B.2.1 Scenario #1: Miller Capacitance is Small

If the Miller capacitor of the transistor (C_μ or C_{gd}) is very small, i.e., $Z_2 \gg$ all the other Z 's, then equation (B.14) can be reduced to

$$Z_{in} = \frac{Z_a \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_a + g_m Z_1 Z_L} \cong \frac{Z_a Z_2}{Z_2} = Z_a \quad (\text{B.16})$$

and we know Z_a is the exact solution of the input impedance of the circuit in Fig. B-5.

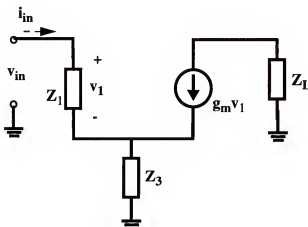


Figure B-5 Small Miller effect approximation

Eq. (B.16) is also the approximation we use throughout Chapter 4. For BJT LNA, this is a very good approximation because modern SiGe BJT has small C_{μ} . For MOS LNA, this is also a good approximation because for a 0.25- μm CMOS process, $C_{gd} \approx \frac{1}{3} C_{gs}$. In scenario #3, it is shown that for cascode LNA's, even when the effect of C_{gd} is included, the input impedance predicted by (B.21) is close to (B.16).

B.2.2 Scenario #2: Miller Theorem

Let us see what happens to (B.14) if there is no degeneration. This is the case of Miller theorem.

If $Z_3 = 0$, then $Z_a = Z_1$ and Eq. (B.14) becomes

$$Z_{in} = \frac{Z_a \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_a + g_m Z_1 Z_L} = \frac{Z_1 \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_1 + g_m Z_1 Z_L} \quad (\text{B.17})$$

Multiplying both the numerator and denominator of Eq. (B.17) by $1/Z_1 Z_2$,

$$Z_{in} = \frac{(1 + Z_L/Z_2)}{\frac{1}{Z_1} \left(1 + \frac{Z_L}{Z_2} \right) + \frac{1}{Z_2} (1 + g_m Z_L)} \quad (\text{B.18})$$

The application of Miller's theorem requires that C_{μ} or C_{gs} must be small so that the current going through it is much smaller compared to $g_m v_1$. This is equivalent to $\left| \frac{Z_L}{Z_2} \right| \ll 1$. Eq. (B.18) becomes

$$Z_{in} \cong \frac{1}{\frac{1}{Z_1} + \frac{1}{Z_2} (1 + g_m Z_L)} = Z_1 \parallel Z_2 \cdot (1 + g_m Z_L) \quad (\text{B.19})$$

in which $Z_2(1+g_m Z_L)$ is the Miller impedance.

B.2.3 Scenario #3: Cascode Circuits

Cascode circuit helps to alleviate the Miller effect by adding a common base/gate transistor between input and output. Z_L is $1/g_{m2}$ instead of the large load seen at the output. g_{m2} is the transconductance of the common base/gate transistor and is very close to $g_{m1}(g_m)$, for BJT LNA $g_{m2} = g_{m1}$; for MOSFET LNA, g_{m2} is slightly less than g_{m1} because the cascode device is often chosen to be smaller than the input device for lower parasitic capacitance at the output and optimal noise match [Flo01]. For simplicity, let us assume $g_{m2} = g_{m1} (g_m)$. Eq. (B.14) becomes

$$Z_{in} = \frac{Z_a \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_a + g_m Z_1 Z_L} = \frac{Z_a \cdot (Z_2 + Z_L)}{Z_2 + Z_L + Z_a + Z_1} \quad (B.20)$$

Also, for cascode circuit, $|Z_L| \ll |Z_2|$ which further reduces (B.20) into

$$Z_{in} \cong \frac{Z_a}{1 + (Z_a + Z_1)/Z_2} \quad (B.21)$$

Equation (B.21) is the input impedance expression for the general cascode circuit. In cascode LNA design, the emitter/source degeneration (Z_3) consists of a small inductor only. Therefore, from Eq (B.15), $Z_a \cong Z_1$, and Eq. (B.21) becomes

$$Z_{in} \cong \frac{Z_1}{1 + 2Z_1/Z_2} = \frac{1}{1/Z_1 + 2/Z_2} \quad (B.22)$$

Eq. (B.22) says that the input impedance is approximately $C_{gs} // 2C_{gd}$ or $C_\pi // 2C_\mu$ for cascode LNA's [Okk02].

APPENDIX C BJT AND MOS LNA NOISE PARAMETERS

C.1 BJT Noise Parameters

The BJT small signal model including noise sources is shown in Fig. C-1.

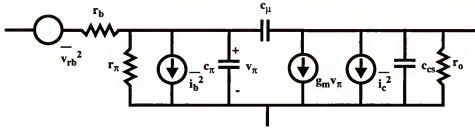


Figure C-1 A BJT small signal model including noise sources

BJT major noise sources include: thermal noise of r_b , $\overline{v_{rb}^2} = 4kTr_b\Delta f$; shot noise associated with the base current or holes jumping over the base-emitter junction $\overline{i_b^2} = 2qI_b\Delta f$; shot noise associated with the collector current or electrons jumping over the base-emitter junction $\overline{i_c^2} = 2qI_c\Delta f$. Putting this model in the BJT cascode LNA, the equivalent input referred noise generators $\overline{v_i^2}$ and $\overline{i_i^2}$ can be found [Okk02]. All the noise parameters can also be derived.

$$\overline{v_i^2} \equiv \frac{i_c^2}{g_b^2} + \overline{v_{rb}^2}, \quad (C.1)$$

where $g_b \equiv g_m \cdot \frac{Z_\pi}{Z_o - j\omega L_b}$ and,

$$\overline{i_i^2} \equiv \frac{i_c^2}{g_m \cdot Z_\pi} + \overline{i_b^2}. \quad (C.2)$$

L_b is usually off-chip and noise-less. The total input referred noise is

$$v_{ni} = v_i + i_i \cdot (Z_o + j\omega L_b) , \quad (C.3)$$

and the noise factor can be expressed as,

$$F = 1 + \frac{\overline{v_{ni}}^2}{\overline{v_s}^2} = 1 + \frac{r_b + \frac{2Z_o^2}{|g_m \cdot Z_\pi|^2} + \frac{g_m \cdot (Z_o^2 + \omega^2 L_b^2)}{2\beta}}{Z_o} . \quad (C.4)$$

The noise parameters F_{min} , G_n , $Z_{opt} = R_{opt} + jX_{opt}$ (impedance form) can be derived once Eqs. (C.1) and (C.2) are found [Okk02].

$$G_n = \frac{g_m}{2|g_m Z_\pi|^2} + \frac{g_m}{2\beta_o} , \quad (C.5)$$

$$X_{opt} = -X_{cor} \cong -\frac{\frac{1}{c\pi\omega}}{1 + \frac{|g_m Z_\pi|^2}{\beta_o}} , \quad (C.6)$$

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_{cor}^2} , \quad (C.7)$$

$$F_{min} = 1 + 2G_n(R_{cor} + R_{opt}) , \quad (C.8)$$

where

$$R_{cor} = r_b + \frac{\beta_o \frac{g_m L_e}{C\pi}}{\beta_o + |g_m Z_\pi|^2} , \quad (C.9)$$

and

$$R_u = r_b + \frac{g_m \left[\left(\frac{g_m L_e}{C_\pi} \right)^2 + (X_\pi - X_e)^2 \right]}{2 \left(|g_m Z_\pi|^2 + \beta_o \right)} . \quad (C.10)$$

C.2 MOS Noise Parameters

The MOS small signal model including noise sources is shown in Fig. C-2. They include thermal noise of gate resistance r_g ,

$$\overline{v_{rg}^2} = 4kTr_g \Delta f , \quad (C.11)$$

gate induced noise

$$\overline{i_g^2} = 4kT\delta \left(\frac{\omega^2 C_{gs}^2}{5g_{do}} \right) \Delta f \quad (C.12)$$

and channel thermal noise

$$\overline{i_d^2} = 4kT\gamma g_{do} \Delta f . \quad (C.13)$$

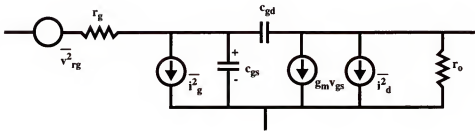


Figure C-2 MOS small signal model with noise sources

From Eqs. (C.11), (C.12) and (C.13), the equivalent input referred noise generators

$\overline{v_i^2}$ and $\overline{i_i^2}$ can be found [Sha97]. Using the admittance form, the noise parameters F_{min} ,

R_n , $Y_{opt} = G_{opt} + j B_{opt}$, can be expressed as

$$R_n = \frac{\gamma}{\alpha \cdot g_m} \quad , \quad (C.14)$$

$$B_{opt} = -\omega C_{gs} \left[1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}} \right] \quad , \quad (C.15)$$

$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5\gamma} (1 - |c|^2)} \quad , \quad (C.16)$$

$$F_{min} = 1 + 2R_n(G_{opt} + G_c) = 1 + 2R_n G_{opt} \quad (C.17)$$

where, $\gamma \sim 2/3$ to 2 , δ is 2γ , $\alpha \sim 1$, and $c \sim 0.395$.

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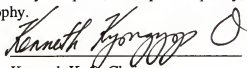
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BIOGRAPHICAL SKETCH

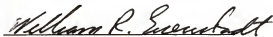
Xi Li was born in Shanghai, China, in August, 1969. He received the B.S. in physics from Peking University in 1991, and the M.S. in electrical and computer engineering from the University of Florida in 1999. Since 1997, he has been working on his graduate degrees in the Silicon Microwave Integrated Circuits and Systems (SiMICS) Research Group, at the Department of Electrical and Computer Engineering of University of Florida. During the summer of 1998, he worked for Rockwell Semiconductor (now Jazz Semiconductor), Newport Beach, California, in the area of semiconductor Bipolar and BiCMOS process development, as a summer intern. During the summer of 1999, he worked for Harris Semiconductor (now Intersil Corporation), Palm Bay, Florida, in the area of RF IC design, as a summer intern. Since 2000, he has been with the Mixed Signal and RF IC design group at Intersil Corporation in Palm Bay, Florida, as an IC design engineer.

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Kenneth K. O., Chairman
Professor of Electrical and
Computer Engineering

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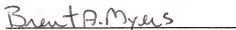
William R. Eisenstadt
Associate Professor of Electrical
and Computer Engineering

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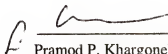


Jonathan C. L. Liu

Associate Professor of Computer
and Information Science and
Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

May, 2003



Pramod P. Khargonekar
Dean, College of Engineering

Winfred M. Phillips
Dean, Graduate School